

# ENGINEERING NOTEBOOK



**CONFIDENTIAL**

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## ENGINEERING NOTEBOOK

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2. Complete each sheet in its entirety, but start a new sheet on every new day that you wish to record information.
3. Date and sign each log sheet.
4. All log sheets containing information that might have particular significance must be signed and dated by one witness who reads the sheet and understands its contents.

NOTE: If there are co-inventors, both should sign in the area marked *WRITER*, and a third party is required to sign as witness.

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1. Use black ink. Do not use blue ink or pencil; it is difficult to reproduce.
2. Do not try to erase. If revisions or changes are necessary, cross out and rewrite. See item 8 of instructions.
3. Clarity is essential but precision drawings are not required; therefore, free-hand sketches are acceptable.

Book No. 7682 Assigned to Joe Dequin

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NUMBER ASSIGNED BY  
STEVE BRISTOL'S OFFICE

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GAME OR PROJECT

STELLA \*

ADJUSTING TO THIS NOTE BOOK COULD BE A PROBLEM. EVERYBODY HAS HIS/HER HABITS, AND MAJOR ADJUSTMENTS ARE DIFFICULT.

ON APRIL 1, 1976 I STARTED A NOTEBOOK. RETROACTIVELY NUMBERED "13" ON 2 FEB 77. VERY LITTLE OF MY DESIGN WORK, OR IDEAS, PARTICULARLY FOR PROGRAMS, IS CONTAINED IN THAT BOOK. I HABITUALLY WORK ON GIVEN "ENGINEERING PADS". ANYTHING WORTH SAYING WINDS UP IN BINDERS.

I SUSPECT THAT THE DOMINANT VALUE OF THIS BOOK IS LEGAL DOCUMENTATION OF PROPRIETARY IDEAS. MY GREEN SHEETS SERVE FINE FOR GETTING THE WORK DONE, BUT I DOUBT THAT THEY WILL STAND UP IN COURT.

ANOTHER FUNCTION OF THIS BOOK MAY BE SO THAT AN "ENGINEERING MANAGER" CAN EVALUATE MY WORK. THIS DOES CONSTITUTE A PROBLEM, SINCE THE LINES OF AUTHORITY HERE ARE NOT CLEAR. I DO WHAT NEEDS TO BE DONE, WITH PRIORITY DETERMINED BY CONSENSUS WITH JAY MINER, LARRY WAGNER, AND BOB BROWN, AND NILES STROHL, THE STELLA PROJECT ENGINEER WITHIN THE CONSUMER PRODUCT ENGINEER GROUP DOWN THE HALL.

IF MICROELECTRONICS FRAGMENTS IN TO A CHIP DEVELOPMENT GROUP AND A SOFTWARE DEVELOPMENT GROUP, MY ROLE WILL BECOME CONFUSED.

THESE ARE MY THOUGHTS ON WHAT SHOULD GO IN HERE; AND IF ANYONE BESIDES BOB BROWN THINKS HE HAS ANYTHING TO SAY ABOUT IT, HE/SHE SHOULD SPEAK UP. I DO REGARD DR. BROWN AS MY BOSS.

\* K NAMED AFTER MY BICYCLE, A STELLA SX-73 10kg bike

2



GAME OR PROJECT

STELLA

WHAT SHOULD GO IN THIS BOOK:

DAILY

SUMMARIES OF IDEAS ABOUT:

NEW SYSTEM ARCHITECTURES, INCLUDING CHIPS.

DEVELOPMENT SYSTEM ARCHITECTURES.

FUNCTIONAL SPECIFICATIONS FOR SOFTWARE:

CHIP DIAGNOSTICS

BOARD DIAGNOSTICS

DEVELOPMENT SYSTEM DIAGNOSTICS.

GAME (APPLICATIONS) SOFTWARE.

~~SOME~~ SOME INTERNAL SPECIFICATIONS FOR ABOVE SOFTWARE.

THOUGHTS AND OBSERVATIONS ABOUT OTHER SYSTEMS, CHIPS SETS (EX: SIGNETICS)

IDEAS FOR GAMES FROM COIN OP

DAILY SUMMARIES OF: PROBLEMS ENCOUNTERED IN DEVELOPMENT SYSTEM WORK.

MAYBE OTHER THINGS, WHEN I THINK OF THEM.

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GAME OR PROJECT

STELLA

PADDLE GAME CODE.

TO DATE A 4 PLAYER 2 PADDLE/PLAYER SOCCER GAME HAS BEEN WRITTEN FOR STELLA.

I AND BOB BANERJEE ARE CONSIDERING IT TO A 4 PLAYFIELD / 16-32 PADDLE CONFIGURATION SYSTEM OF VERTICAL PADDLE GAMES. THIS GAME SET WILL BE SUBMITTED TO THE GROUP FOR PLAY - WORKING OUT - AND COMMENTS. IT WILL USE BOTH OPTIME AND GAME SELECTS.

AFTER COMMENTS IT WILL BE BOILED DOWN INTO A SPECIFIC GAME SET, USING GAME SELECT ONLY.

THAT A SET OF PADDLE GAMES INCORPORATING HORIZONTAL PADDLES, INCLUDING BASKETBALL, QUADRUPODS, AND VOLLEYBALL (REBOUND) WILL BE PURSUED. (I WOULD HOPE THAT MR. BANERJEE GETS TO DO THIS).

I WILL THEN PURSUE BREAK OUT, PIN PONGS (a la ACLETTA), AND A WHEELS GAME FOR SEARS.

AFTER THAT, I DON'T KNOW.

I WILL BE TRAINING NEW ~~NEW~~ PEOPLE AS PROGRAMMERS AND ~~FOR~~ FOR HARDWARE SUPPORT.

I WILL HELP JAY, STEVE MAYER, AND KAREY WAGNER TO ARCHITECT A FOLLOW ON TO STELLA.

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WRITER

JESUR

DATE

2 FEB 77

WITNESS

David H. Miller

DATE





GAME OR PROJECT

STELLA

3RD, 4TH FEBRUARY - WROTE AND  
 DEBUGGED ATTRACT MODE CODE,  
 INSTALLED GAME NUMBER DEPENDANT  
 PLAYFIELD AND COLORS. E/W SWITCH  
 SOFTWARE.

MONDAY & TUESDAY 7TH, 8TH FEBRUARY  
 MOST TIME SPENT FIRE FIGHTING.

NILES STROHL DESIGNED AND INSTALLED  
 A MODIFICATION TO KIM DEVELOPMENT  
 SYSTEM THAT MIXES SOUND IN WITH  
 VIDEO → INTO TV SPEAKER. IT WORKS  
 SATISFACTORILY, W/O SERIOUSLY DEGRADING  
 LOW FREQUENCY RESPONSE OF AUDIO.

SOME KINDS OF SERIOUS PROBLEMS ARE  
 OCCURRING BETWEEN THE BREADBOARD AND  
 LARRY WAGNER'S PROGRAMS. SOME FAULTS  
 TRACE TO KIM SYSTEM RAMS, BUT THESE  
 ARE INDEPENDANT.

WEDNESDAY, THURSDAY, FRIDAY. 9, 10, 11 FEB.  
 NUBS & BOLTS STUFF,  
 GETTING STELLA READY FOR MARKET TESTING.

MONDAY 14 FEB MORE OF SAME.

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WRITER

DECTUR

DATE

WITNESS

DATE



GAME OR PROJECT

STELLA

15 FEB NOTES ON READING ABOUT GI TANK AND  
OTHER CHIPS IN THE GI BOOK

OBJECT RESOLUTION LOOKS COARSE FROM THE SPECS.  
"8/100" OF SCREEN VS 8/160 FOR STELLA

~~16~~ MOTION SOUNDS FINER. "32 ROTATIONS"  
"32 DIRECTIONS"  
VS 16 ROTATIONS AND DIRECTIONS FOR STELLA.

~~3~~ 3 FORWARD AND 3 REVERSE SPEEDS  
REVERSE SOUNDS USEFUL - BUT I  
DON'T KNOW ABOUT MULTIPLE SPEEDS -  
THEY'RE EASY TO DO WITH THE  
TIME FEATURE

THEY HAVE MINES, AND THEY HAVE BULLET  
EXPRESSIONS.

SCORING - ~~10~~ IN GI - GAME ENDS AT 31.  
USE - GAME ENDS AT 10  
- WE COULD INCREASE UPPER LIMITS  
OF SCORE. BUT IT MIGHT JUST  
INCREASE LENGTH OF GAME

WE DON'T HAVE A GENERAL PURPOSE  
MICRO PROGRAMMABLE CHIP, TO ~~CREATE~~  
GENERATE SINGLE CHIP GAMES.

MOS TECHNOLOGY'S GAME CHIP, AND  
ARLITE ARE BOTH EXAMPLES OF SUCH  
A DEVICE. WE OUGHT TO CONSIDER  
SUCH A MACHINE FOR A 1978 PRODUCT.

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GAME OR PROJECT

STELLA

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FOR EXAMPLE,

WHY NOT LOOK AT THE  
MOS TECHNOLOGY 650X / ATARI TIA ~~TRIO~~  
/ 6532 TRIO.

DESIGN A SPECIAL PURPOSE ~~TRIO~~  
MACHINE THAT EXECUTES A MICRO CODE -  
(PERHAPS IN AN EXTENDED ROM) ~~TRIO~~ WHICH  
IS (AT A FLOW CHART LEVEL) SIMILAR TO  
THAT EXECUTED BY STELLA PROGRAMS.  
- EXCEPT THAT THERE ARE FEWER VARIABLES  
- AND MORE SPECIAL PURPOSE INSTRUCTIONS:

EX: RIGHT NOW THE 6507 DRAWS THE  
TANK GRAPHICS LINE PAIR BY LINE PAIR

SUPPOSE A MICRO PROGRAMMING MACHINE  
HAS A REGISTER FOR OBJECT X VERTICAL  
POSITION, AND A REGISTER FOR OBJECT X  
DISPLAY, AND AN  $N \times N$  ~~BIT~~ BIT PATTERN  
FOR OBJECT X GRAPHICS.

A SINGLE INSTRUCTION MIGHT  
DO A COMPARISON OF VPOS AND LINE COUNT.  
AND DECIDE RANGE, AND INDEX TO GRAPHICS.  
A SECOND INSTRUCTION WOULD BRANCH ON RANGE.  
A THIRD INSTRUCTION WOULD LEAD DATA INTO  
GRAPHICS.

PLAYFIELD COULD BE A RESIDENT ROM.

~~STELLA~~  
ETC.

GAME OR PROJECT

NEW PROJECTS FOR 78 / PADDLE GAMES.

THE BASIC IDEAS - I SUSPECT, IS

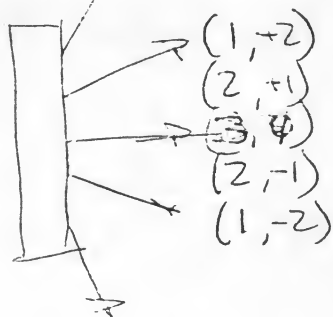
TO GO FOR THE MIDDLE GROUND BY BUILDING SINGLE CUSTOM (+MATHS STD RANG/PARS) WHICH ~~CAN~~ CAN DO SMALL (40) SET OF GAMES. - TAKE SUCH SYSTEM FUNCTIONS AND ~~REPAIRING~~ REPAIRING INTO ARCADE LIKE SYSTEMS.

**BALL / PADDLE INTERACTION ALGORITHMS,**

1) SIMPLE.  $|HM| = 1$ .  
 SIGN(HM) = FUNCTION OF PLAYER #.  
 VM = FUNCTION OF IMPACT POINT -2 - +2

2)  $|HM| = 1, 2, 3$   
 $\#HITS = \phi, 1, 2, 3 \Rightarrow 1$   
 $\#HITS = 4, 5, 6, 7 \Rightarrow 2$   
 $\#HITS \geq 8 \Rightarrow 3$   
 SIGN = FUNCTION OF PLAYER #,  
 VM = FUNCTION OF IMPACT POINT.

3)  $|HM|, VM =$  FUNCTION OF IMPACT POINT.



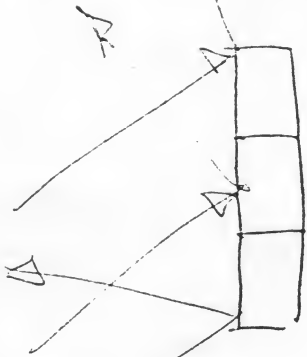
SIGN HM  $\leftarrow$  PLAYER #.

HM	VM
+2	1
+1	1
0	2
-1	1
-2	1

GAME OR PROJECT

PADDLE GAMES

4) "ENGLISH"  
 $(|H_M|, V_M) = f(\text{IMPACT PT})$



$V_M = V_M + 1$	$ H_M  =  H_M  - 1$
$V_M = V_M$	$ H_M  =  H_M $
$V_M = V_M - 1$	$ H_M  =  H_M  + 1$

$H_M = 1, 2, 3, -1, -2, -3$        $V_M =$

SUMMARY:

	$ H_M  =$	$V_M =$
1)	$H_M$	$f(\text{IMPACT PT})$ $-2 \leq V_M \leq +2$
2)	$f(\# \text{ OF HITS})$ $-3 \leq H_M \leq +3$ and $\neq 0$	$f(\text{IMPACT PT})$ $-2 \leq V_M \leq +2$
3)	$f(\text{IMPACT PT})$	$f(\text{IMPACT PT})$ $-2 \leq V_M \leq +2$
4)	$f(\text{IMPACT PT}, H_M)$	$f(\text{IMPACT PT}, V_M)$

AUDIO VOLUME =  $|H_M| \times f.$

$OR = |H_M| + |V_M| \times 2$

OR  $\Rightarrow$  FUNCTION OF IMPACT PT.

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GAME OR PROJECT

NEW MACHINES

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IF 11 PINS ARE USED ON A SCHEM MAP  
TO CONTROL A ~~RAM~~ DYNAMIC RAM (DRAM).  
ARRAY. - IT HAS 13 LEFT IN A 28 PIN  
PACKAGE, AND 29 LEFT IN A 40 PIN.

AS A MINIMUM ADDED AN EXISTING STRUKA,  
IT NEEDS:

	2	+5, GND	
	2	OSC IN, $\phi$ 2 IN	
	8	D $\phi$ - D7	
9-10	2-3	CHIP SELECTS.	} 8 minimum
		<del>1</del> RW	
		3-6 ADDRESS LINES	
	21-22	LINES	
	<del>1</del>	<del>RAM CONTROL</del>	
	1-4	VIDEO OUT (1 IF PIPED INTO STRUKA, 4 IF CHROMA (LUM IN))	
	22-26		
	+ 11	RAM CONTROL	
	33-37	$\Rightarrow$ 40 PINS	

IF THIS IS A STAND ~~ALONE~~ ALONE  
SYSTEM -

DELETE A CHIP SELECT. ~~AD~~  
ADD A COLOR DELAY INPUT. ~~AND A  $\phi$ 2 IN~~  
ADD A  $\phi$ 0 OUTPUT  
ADD A  $\overline{RDQ}$  OR RDY OUTPUT  
ADD ~~1~~ 2 AUDIO OUTPUTS.  
ADD 1 BANK OUTPUT 0

4-5  
~~33~~ 37  
41-42 !!

GAME OR PROJECT

NEW MACHINES

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TIA: GND  
 SYN  
 RDY  
 $\phi$  OUT  
 L1  
 B  
 L2  
 L $\phi$   
 COL  
 DEL  
 OSC  
 AM1  
 AM $\phi$   
 D $\phi$   
 D1  
 D2  
 D3  
 D4  
 D5  
 +5  
~~CS3~~  
~~CS2~~  
~~CS1~~  
~~CS $\phi$~~   
 RW  
 $\phi$  2 IN  
 A5  
 A4  
 A3  
 A2  
 A1  
 A $\phi$   
 D $\phi$   
 D7

DEPENDENT:  
 SCOUT  
 MAP

GND  
 SYN  
 RDY or IRQ  
 $\phi$  OUT  
 L1  
 B (?)  
 L2  
 L $\phi$  (?)  
 COL  
 DEL  
 OSC  
 AM1  
 X  
 D $\phi$   
 D1  
 D2  
 D3  
 D4  
 D5  
 +5  
~~CS3~~  
~~CS2~~  
~~CS1~~  
~~CS $\phi$~~   
 RW  
 $\phi$  2 IN  
 {A5 }?  
 {A4 }?  
 A3  
 A2  
 A1  
 A $\phi$   
 D $\phi$   
 D7  
 X

27  
 +11  
 38

Le IHATS.

GAME OR PROJECT  
 NEW MACHINES

ADD ON CHARACTER CHIP TO TIA

IT COULD FIT INTO THE SAME MEMORY SPACE AS THE TIA:

19 WRITE ADDRESSES FROM (2D TO 3F)

$$\begin{array}{r} 3F \\ 2C \\ \hline 13H = 19 \end{array}$$

~~19 READ ADDRESSES~~

OR USE ONE CHIP SELECT ON AB6 TO DISTINGUISH IF FROM STRLA - GIVING IT 64 R/W ADDRESSES.

COULD USE THE RDY LINE IN PARALLEL WITH TIA FOR RESYNCHRONIZATION - OR HAVE MICRO DO THAT ITSELF W/TIA.

~~PIPS~~ COULD ENCODE ITS OUTPUT INTO TIA ON ONE OR TWO LINES, OR MIX THEM EXTERNALLY BY WIRED OR ON CHIPMA AND LUM LINES.

2 +5, GND

2 φ2, OSC

8 D0 - D7

8 { 2 CHIP SELECTS AND 6 ADDRESS LINES AND NO R/W

~~6-10~~ 3 CHIP SELECTS, AND 3 ADDR - 6 ADDRESS LINES AND R/W

28-30

+ UNUSED OUTPUTS

1-4

1-2 OR INTO TIA OR 3-4 VIDEO OUTPUTS

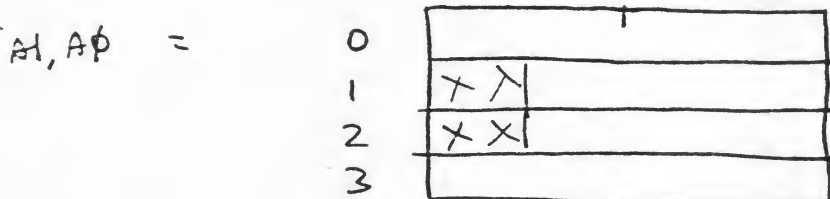
28-34

TOTAL PINS.

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GAME OR PROJECT  
 NEW MACHINES.

SUPPOSE USE 4 WRITE ADDRESSES ONLY.



CONTROL WORD  
 SHIFT REGISTER DATA - WRITE 20 TIMES.  
 WRITABLE CHARACTER ADDRESS  
 WRITABLE CHARACTER DATA.

PUT IN LOCATIONS 40-7F<sub>H</sub> REDUNDANTLY.

CS0 = ~~A0~~ A12

CS1 = A7

CS2 = A6

A1 = A1

A0 = A0

5 LINES CS/AD.

2 POWER

2 CLOCKS

8 DATA

17 PINS,

7 PINS FOR OUTPUT.

24 PIN PACKAGE.

EX. 1 LINE INTO TIA. - COLU  
 OR 1 LINE INTO TBA FOR TURN OFF  
 3 CUM, 1 CHR, 1 CTRL.

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- 3 IDEAS :
- 1) 3 LEVEL SCREEN MAPPING
  - 2) 3) DISPLAYING NUMBERS, CHARACTERS
  - 3) SCANNING A KEYBOARD.

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- 1) 3 LEVEL SCREEN MAP IS NECESSARY FOR BOARD GAMES, DOMINOS, ~~OTHERS~~ OTHELLO, CHECKERS, AND OTHERS.

STELLA MAZUR'S IDEA IS TO WRITE ALTERNATE IMAGES ON ALTERNATE FRAMES, SO THAT THE TOTAL SCREEN IS WRITTEN EVERY ~~2~~ 2 FRAMES.

3 LEVELS

- PF. WRITTEN ODD FRAMES
- BACKGROUND
- ~~BACKGROUND~~ PF. WRITTEN EVEN FRAMES

(1A)

LARRY ~~KA~~ KAPLAN'S IDEA: TWO LEVEL SCREEN MAP.

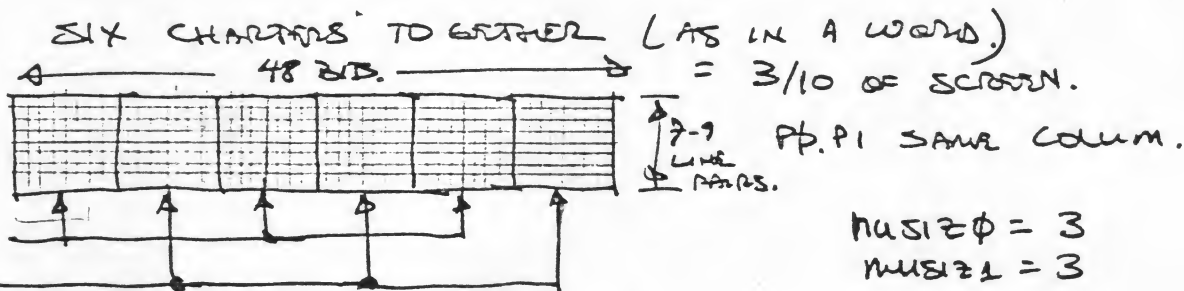
- 1) TURN OFF OBJECTS.
- 2) WRITE <sup>RIGHT</sup> SIDE OF PLAYFIELD ON ONE FRAME, WITH  $COLUP0 = \phi$ ,  $COLUP1 = \text{SOME COLOR}$
- 3) 2ND FRAME, WRITE LEFT SIDE,  $COLUP1 = \phi$ ,  $COLUBK = \text{SAME COLOR}$

CARE SHOULD BE TAKEN IN THE MIXING OF ~~OBJ~~ PF COLOR AND BACKGROUND COLOR

GAME OR PROJECT

FEASIBILITY STUDY IDEAS:

2)A DISPLAYING NUMBERS.. CHARACTERS.

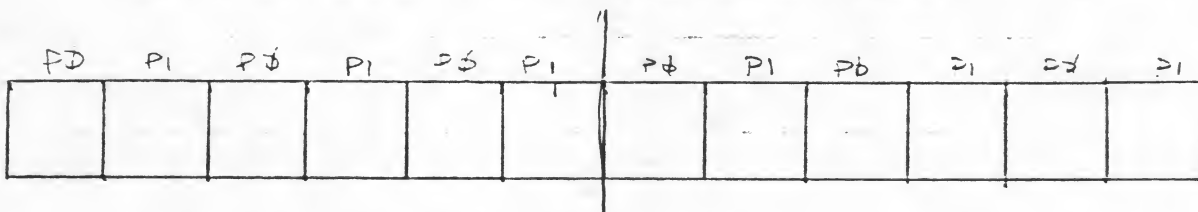


42 BYTES OF IMAGE. WRITTEN OUT REAL FAST.  
 6 BYTES / LINE.

~~5x7~~ (5x7) DOT MATRIX CHARACTERS.  
 6 to 8 (DEPENDENT ON SPACE BETWEEN CHARACTERS)

IF YOU USE LARRY KAPLAN'S IDEA.

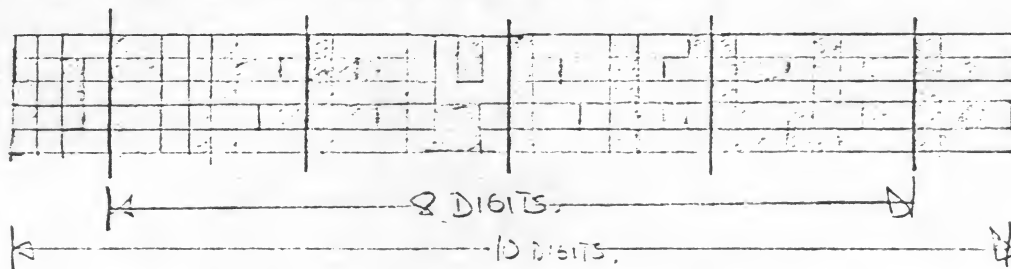
2B)



DO THE SAME THING, EXCEPT WRITE THE LEFT SIX BYTES ON ONE FRAME, AND THE RIGHT SIX BYTES THE NEXT FRAME.

3A) DISPLAY NUMBERS. AS 5x3 MATRICES. —  
 AS IN SCORE MODE NOW.

FUTURE USING PLAYFIELD NOW:



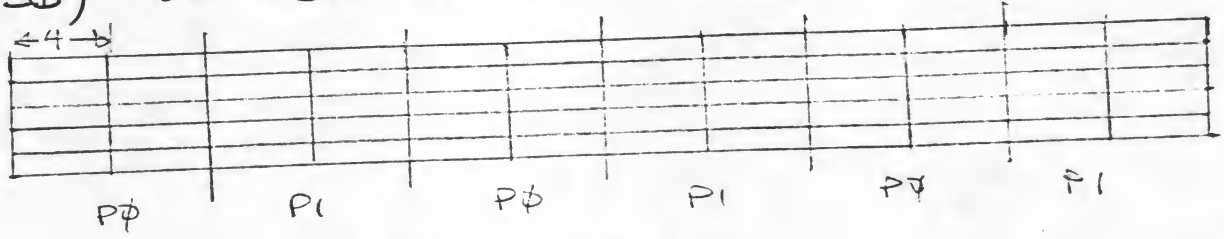
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18

GAME OR PROJECT  
**FEASIBILITY IDEAS**

3b) OR USE PLAYS TO DISPLAY NUMBERS

SURE  
 FEED

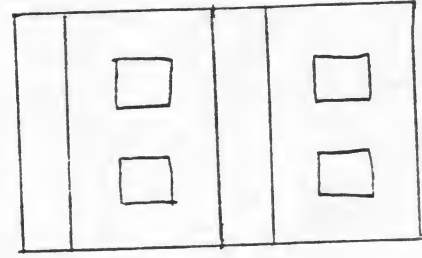
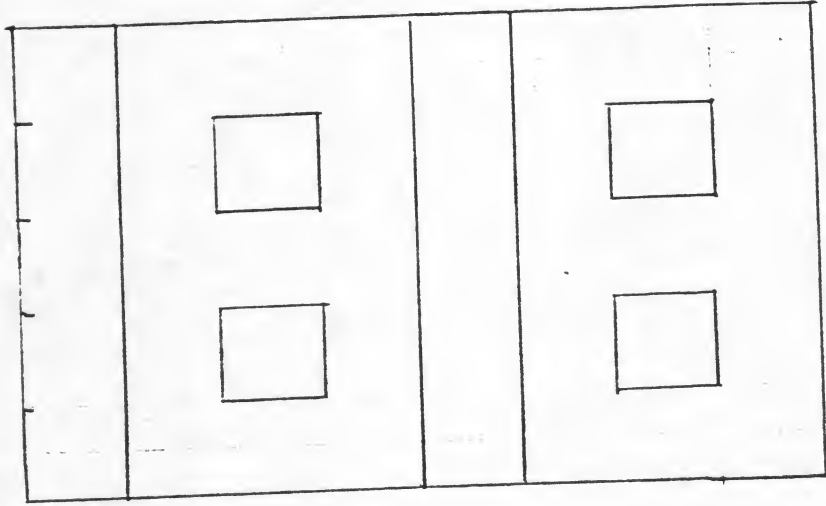


12 SMALL DIGITS.

OR 2 LARGER PAIRS

1 PLAYER  
 X4

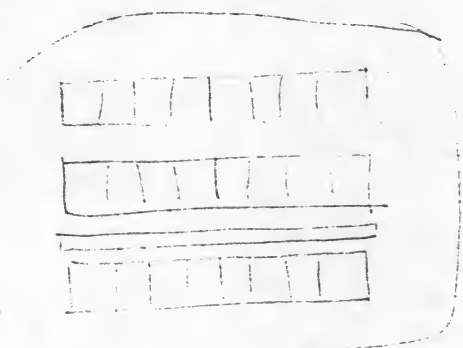
A  
 LINES  
 A



1 PLAYER  
 X2

ALL THIS IS GOOD FOR DISPLAYING SMALLER  
 NUMBERS HERE AND THERE, OR EVEN

FOR IMPLEMENTING A CALCULATOR: !?



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GAME OR PROJECT

FEASIBILITY IDEAS.

## 4) KEYPAD.

THE CONTROLLERS HAVE A LOT OF LINES.

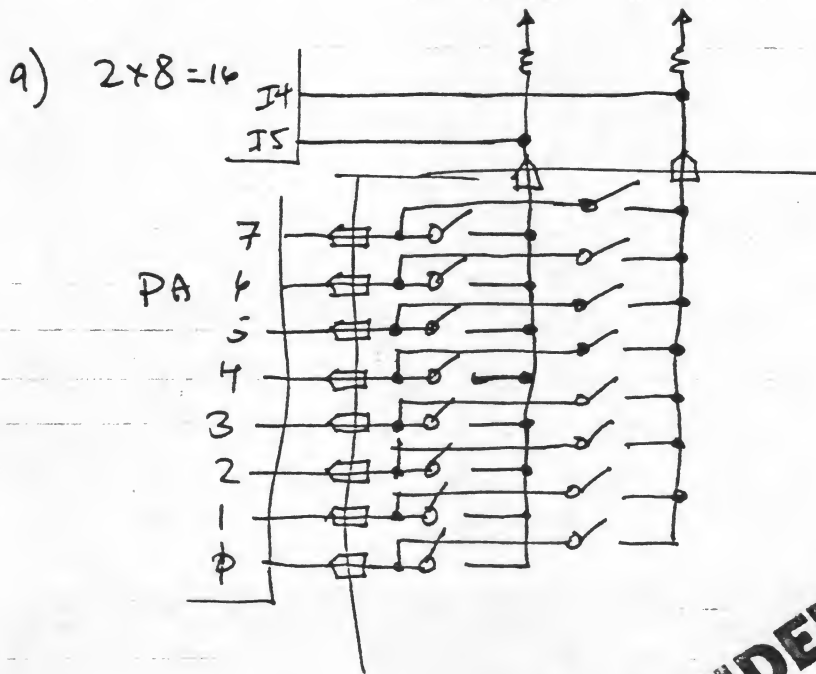
1 8 BIT BIDIRECTIONAL PORT (NOT TRISTATE)

2 TIA INPUT PORTS - HIGH IMPEDANCE (PULLUPS INSIDE)

4 POT PORTS - (SLOW)

14 LINES

SEVERAL MATRICES:

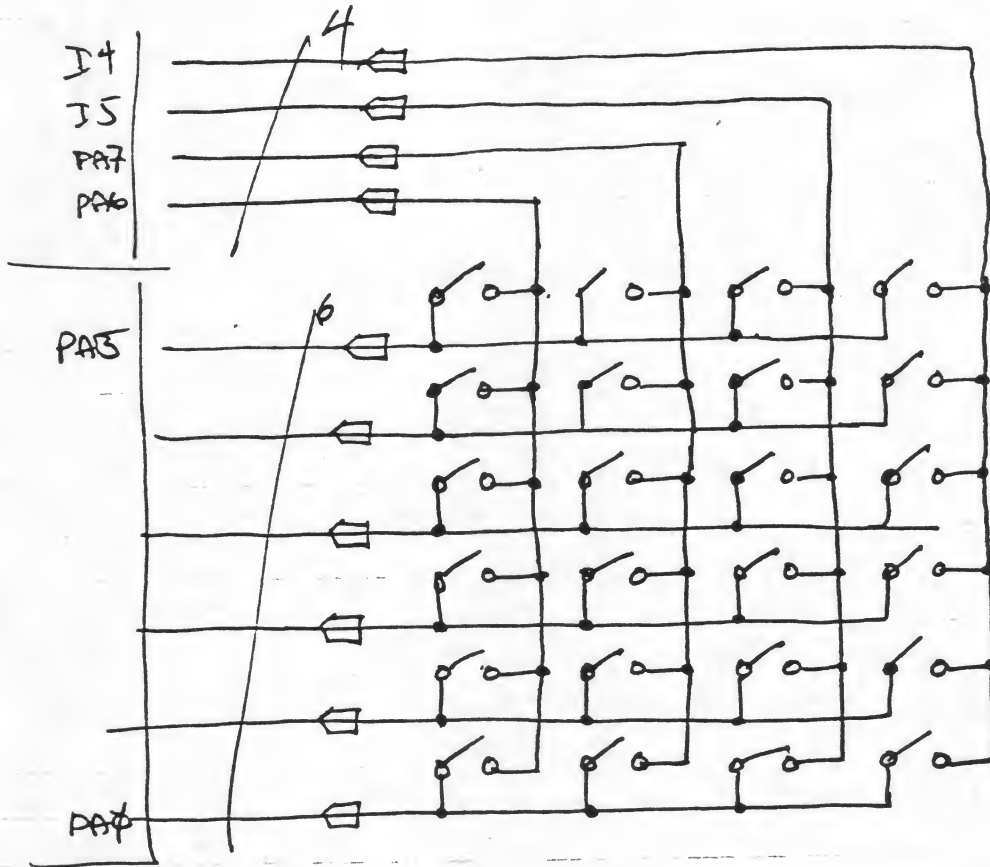


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GAME OR PROJECT  
FEASIBILITY IDEAS

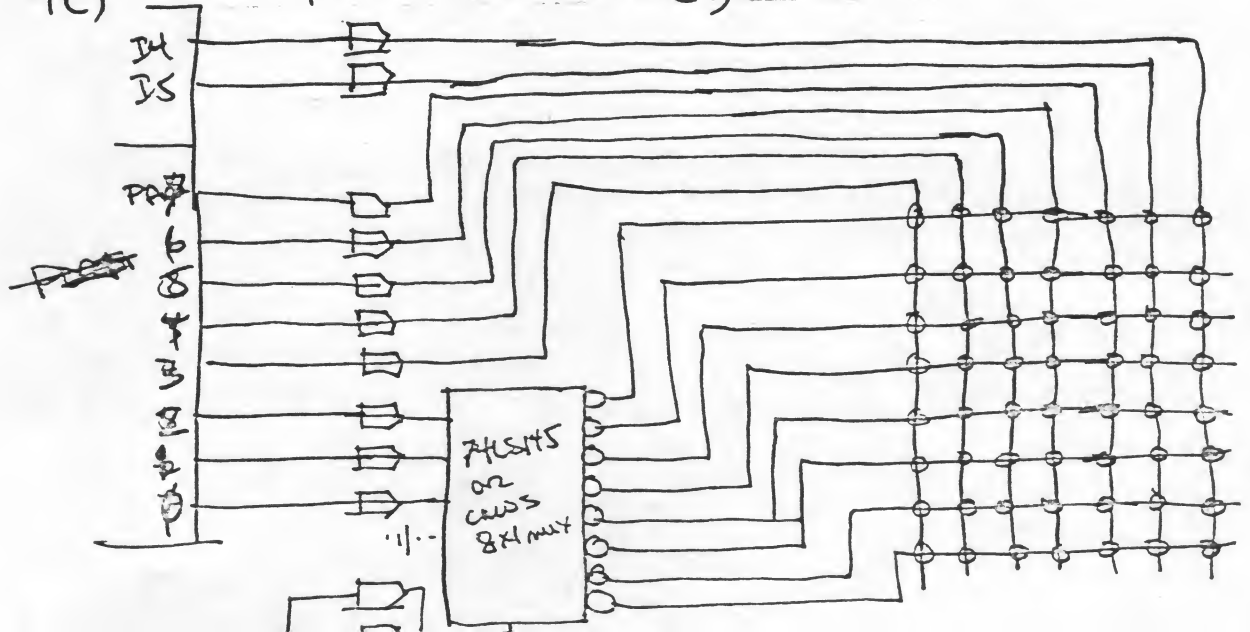
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4b)  $4 \times 6 = 24$



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4c)  $7 \times 8 = 56$  KEYS (!!)



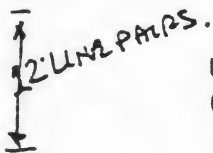
GAME OR PROJECT

NEW GAMES.

5) SOMEBODY, SOMEBODY WENT TO DO MIDWAY GOLFIGHT.



PP



USE BALL AS MOVING TARGET -



(BONUS) ADDING IF YOU HIT IT. LIKE IN CROSSFIRE



USE PLAYFIELD AS FIXED OBSTACLES.



P!

8x12 GRAPHICS.



6,7,8) STEEPLECHASE  
SPACE RACE  
DOMINOS  
FLYBALL  
ETC.

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BACK TO PADDLE GAMES:

BARRIERS

- HOCKEY
- SOCCER
- PONG (TENNIS)
- HANDBALL

DIFFERENT PADDLE CONFIGURATIONS.

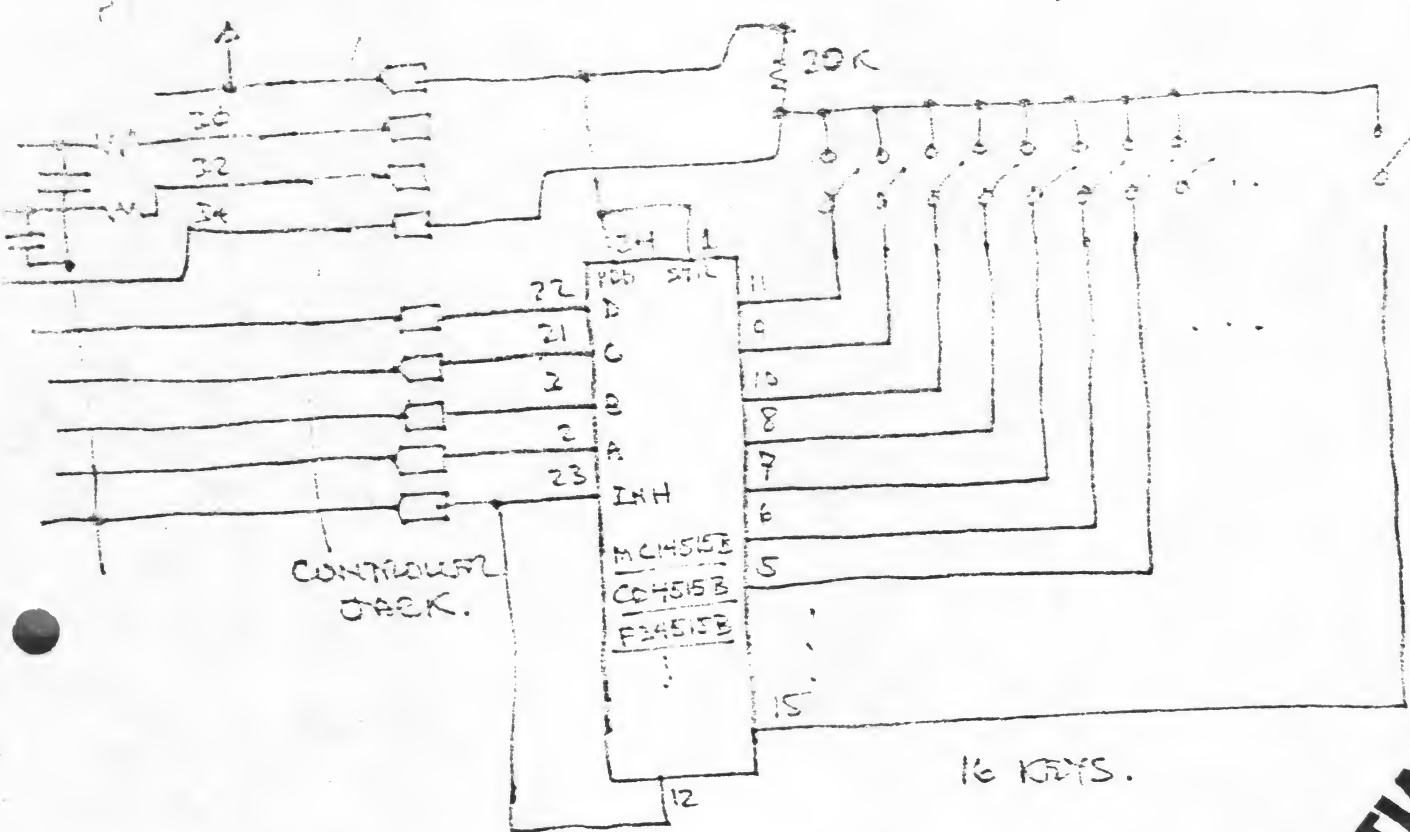
ADD GRAVITY TO HANDBALL?

- BASKETBALL
- VOLLEYBALL
- QUADROPONG.



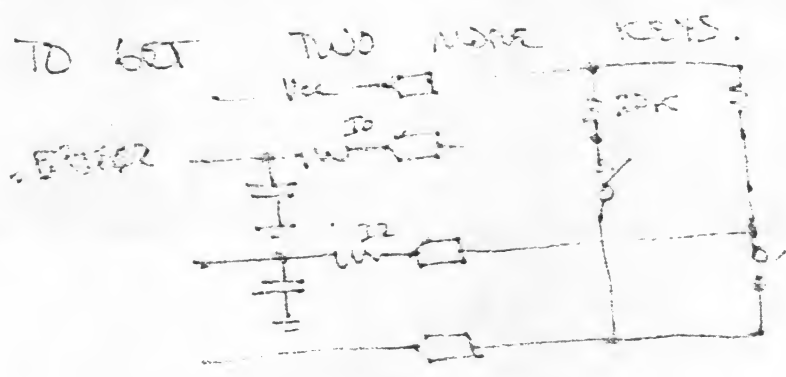
22

GAME OR PROJECT  
STELLA - 16 KEY KEYBOARD.



-3)

$$\frac{5V \times .068 \mu F}{.4 mA} = \frac{5V \times .17 MF}{A} = \frac{.85 msec}{64 \mu sec/line}$$



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TO GET TWO MORE KEYS.  
 SCAN THIS POT  
 WITH THE  
 END OF A  
 FRAME  
 BEFORE TYPING  
 ON KEYS







GAME OR PROJECT  
STELLA -

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REMEMBER TO WRITE DOWN  
MY ATC PROGRAM SOLUTIONS.

IN ATSMART MODE, FOR STELLA GAMES,  
GENERATE SLOW COUNTER,  
AND USE IT TO TOGGLE ALL  
COLOR AND LUMINANCE BITS TO  
RACK POINT, SO THAT <sup>ALL</sup> ~~THE~~ PLACES  
ON SCREEN ~~GET~~ ~~ON~~ ~~ALL~~  
POSSIBLE LUMINANCE AND CHROMA VALUES,  
RANDOMLY DISTRIBUTED, SO THAT  
THE TV DOESN'T GET BURNED IN.

CHARACTERIZE COLOR DELAY LINE

$V_{DEL} = V_{CE} = 5.02$

BURST DUTY CYCLE =  $25/55 = 45\%$   
GREEN (FND) DUTY CYCLE =  $20/55 = 36\%$

$V_{DEL} = 5.65$   
 $= 3.02$   
 $= 4.51$

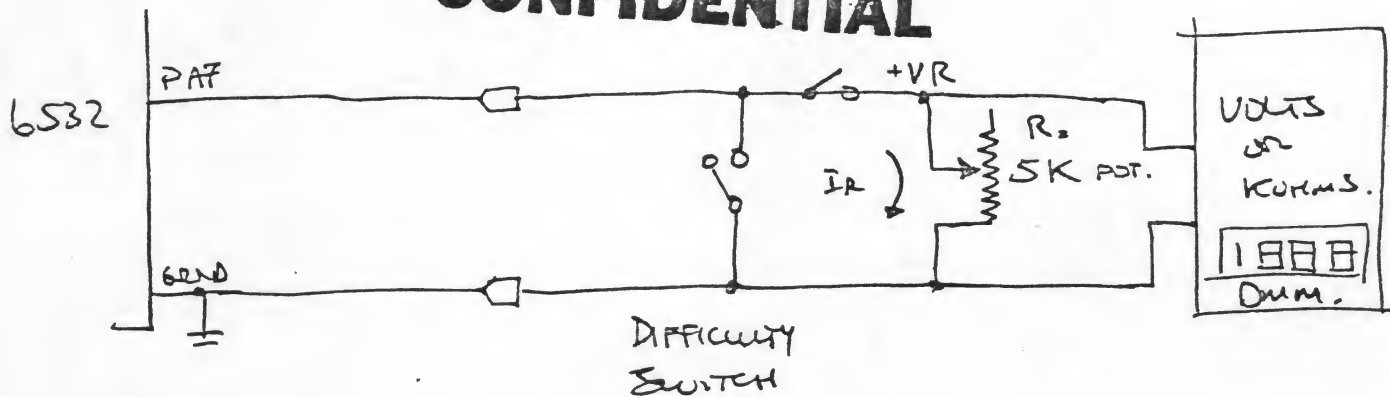
GREEN DELAY = 230 nsec  
" " = 280 nsec  
" " = 330 nsec

CHARACTERIZE	SCHMIDT	TRIGGER	INPUT PULSES
$V_{EC} =$	4.6V	5.03	5.4V
RISE THRESHOLD	1.90	2.02	2.05
FALL THRESHOLD	1.42	1.45	1.45

GAME OR PROJECT

STELLA - 6532 PORTS - CHARACTERIZATION.

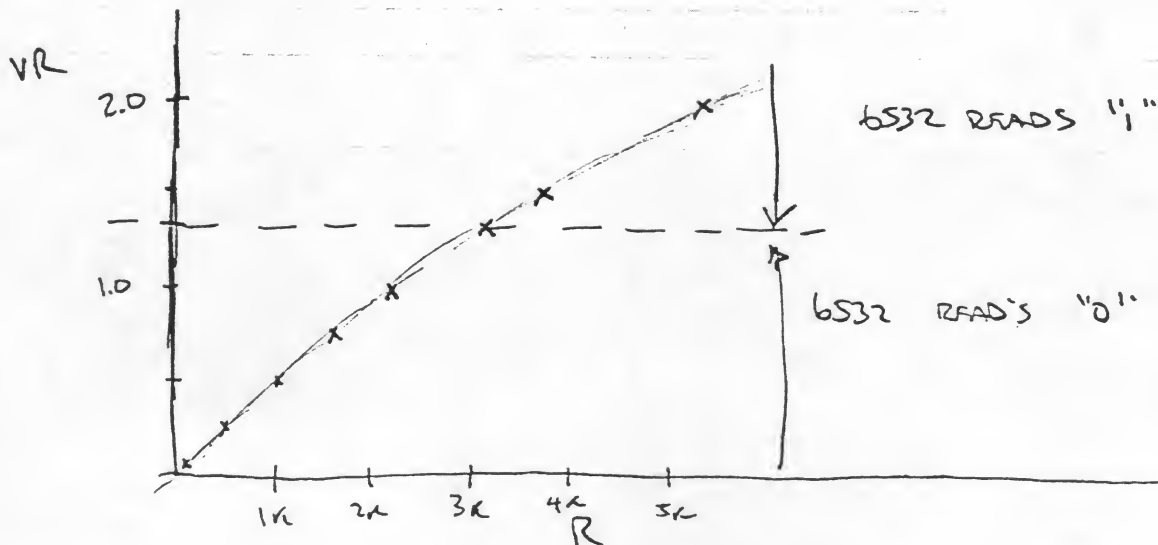
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IR	VR	R
.53 mA	.006	.000
.476 mA	.10	.21K
.480	.25	.52K
.476	.50	1.05K
.465	.75	1.61K
.446	1.00	2.24K
.442	1.33	3.15K
.412	1.50	3.64K
.376 mA	2.00	5.32K

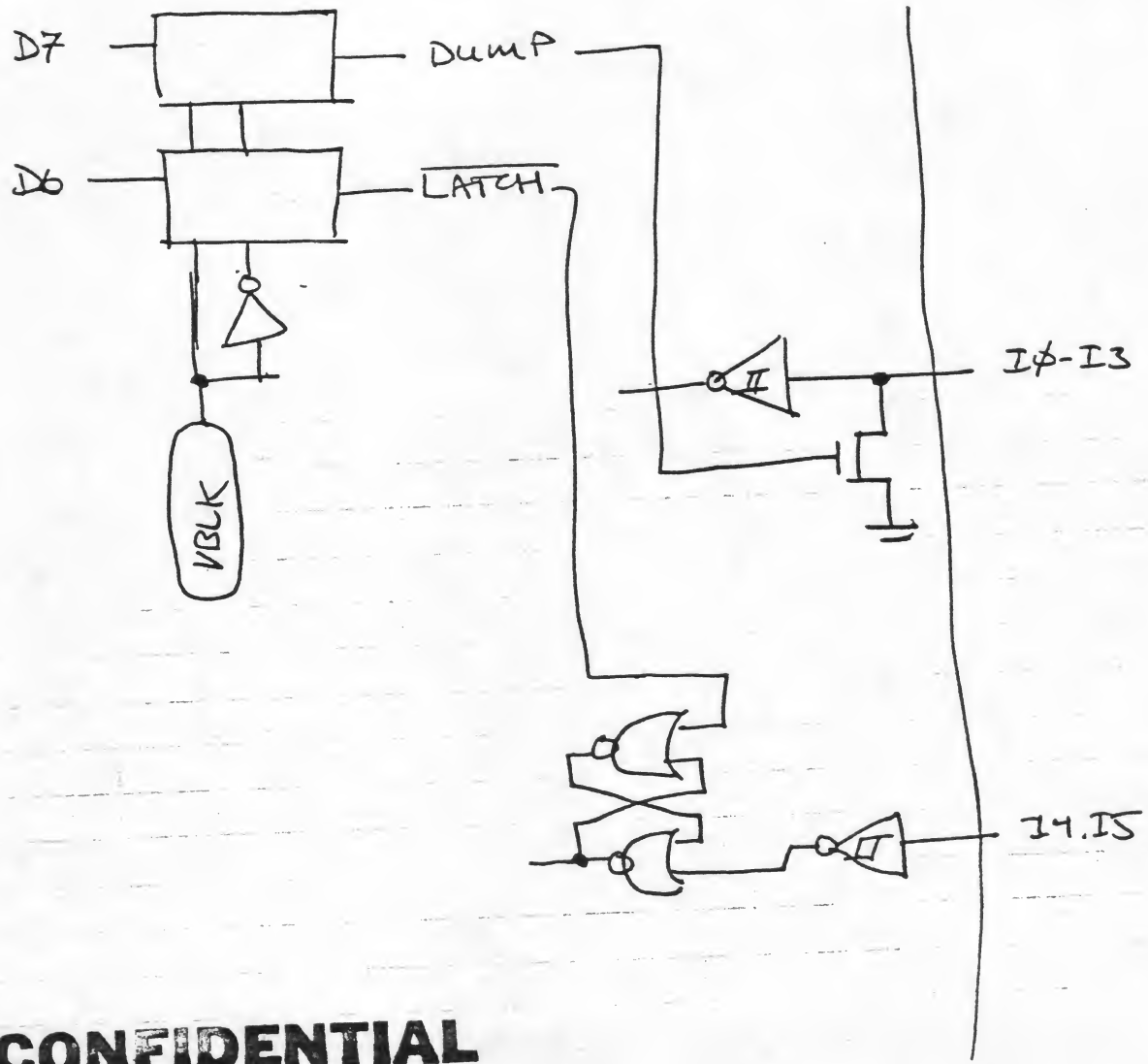
VIRTUALITY NO  
HYSTERESIS OBSERVED  
IN 6532 PORT.

← PB7 THRESHOLD.



GAME OR PROJECT

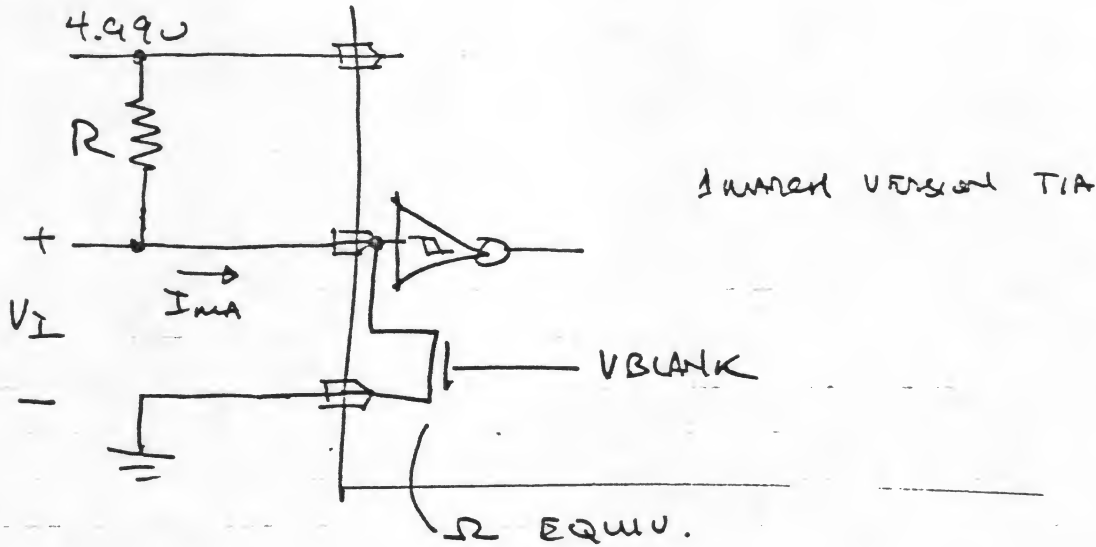
STELLA - CHANGES TO CHIP.



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GAME OR PROJECT

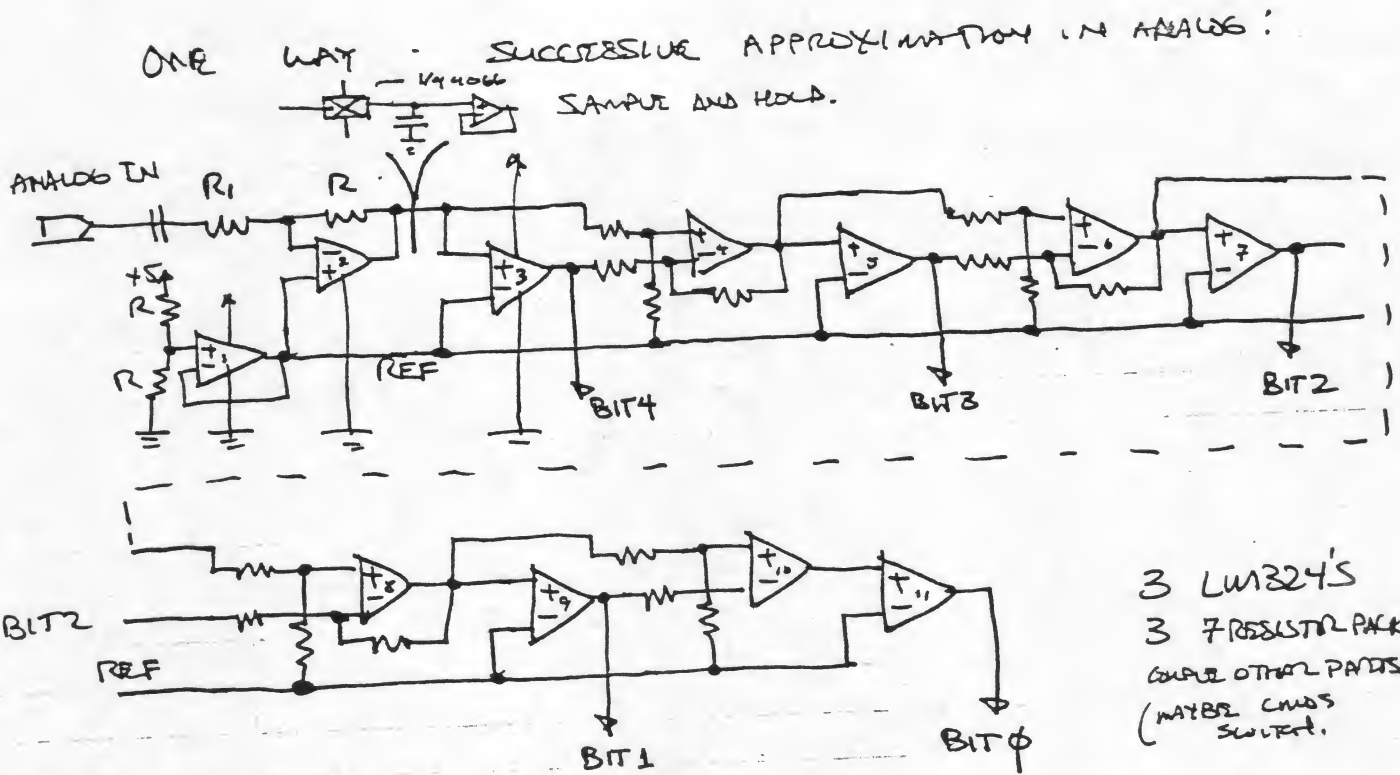
STELLA - CHARACTERIZE PORT PUDDOWN.



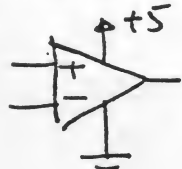
R(k)	V <sub>I</sub>	I (mA)	$\Omega$ equiv.
4.71	.305	.995	306
3.87	.357	1.197	298
3.28	.407	1.397	291
2.67	.489	1.686	290
2.16	.588	2.038	289
1.78	.698	2.411	289
1.48	.824	2.815	292
1.18	1.010	3.373	299
.99	1.192	3.836	311

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PROBLEM. HOW TO DO FAST 5 BIT  
A-D W/ SINGLE SUPPLY AVAILABLE. & A  
CONTROLLER INPUT.



ALL AMPLIFIERS ARE, SAY NATIONAL LM324'S



THIS IS ANALOG SUCCESSIVE APPROXIMATION.  
(ASYNCHRONOUS)

MIGHT NEED SAMPLING, W/ 1/2TA AMP  
AND CMOS SWITCH.

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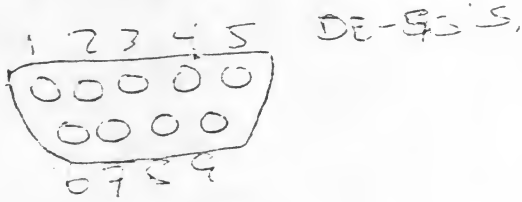




30

GAME OR PROJECT

STELLA



14 APR 77

- |   |                |              |
|---|----------------|--------------|
| 1 | FORWARD,       | PA 4, $\phi$ |
| 2 | BACK           | PA 5, 1      |
| 3 | LEFT           | PA 6, 2      |
| 4 | RIGHT          | PA 7, 3      |
| 5 | POT $\phi$ , 2 |              |
| 6 | TRIGGER,       | I4, IS       |
| 7 | VCC            |              |
| 8 | GROUND         |              |
| 9 | POT 1, 3       |              |

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32



ENGINEERING LOG SHEET

GAME OR PROJECT

IN THE UNITED STATES OF AMERICA  
FIRST INVENTION BY  
LINDSEY PAFF M.P.C. BY THE ATARI CORP.

**CONFIDENTIAL**

GAME OR PROJECT  
NES TECHNOLOGY 3000572

WILL WRITE OUT FIRST, THEN ASSEMBLY,  
BUT FIRST.

6600 FINAL SPEC  
VIC  
PARTS TO WORK WITH  
07-32  
16 BIT. 6509  
VIC W/RESPECT TO ~~DATA~~ ADDA

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6600 - \$10 AR FOR

FEBRUARY, MARCH PARTS.  
PRODUCTION APRIL, MAY.

CPU - SAVES + INSTRUCTIONS  
TO RUN I/O POINTS.

DECREMENT MODULUS INSTRUCTION!!!

REGISTER IN DIRECT ADDRESSING MODE  
AUTO DECREMENT W/ 16 BIT TIMER

TRYING TO OPTIMIZE THIS TO RUN VIC,

ROM/RAM ACCESS. (COMMON DECODE)  
2K + 64

EXTERNAL MEMORY,

3 BIT FC

WORKING  
THIS WILL  
BE 240

GAME OR PROJECT  
M.E.S. TECHNOLOGY

CONFIDENTIAL

6800 - could do a trace

with 40 pins.

may want to find  
space for dedicated chips

(NOTE: PREPARE LOTS OF ANSWERS)  
PAL  
6800 + TIA  
6537 + 6810 + TIA.  
ETC.

6509 "MORE OF A COMPUTER"

VIC REQUIRES ~200 SOME USER ACCESS.

SYSTEM

CPU  
6520 (?)

VIC. CHARACTERIZATION 6540  
RAMS + I/O'S (4 SSI)  
NTSC, PAL or SECAM.

VIC DOES  
ON BOARD  
VIDEO  
SIGNALS

BIG AUDIO SYNTHESIZER

SAMPLES @ END SEPTEMBER.

OR BUY EVALUATOR BOARD

\$45 FOR CPU SET



GAME OR PROJECT

WEST BOUNDARY

in ~~the~~ ~~area~~

check on 30

not check and cover

DIFFERENT DRIVE UNIT OF 14.300 MHz

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WRITER

DATE

WITNESS

DATE

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36

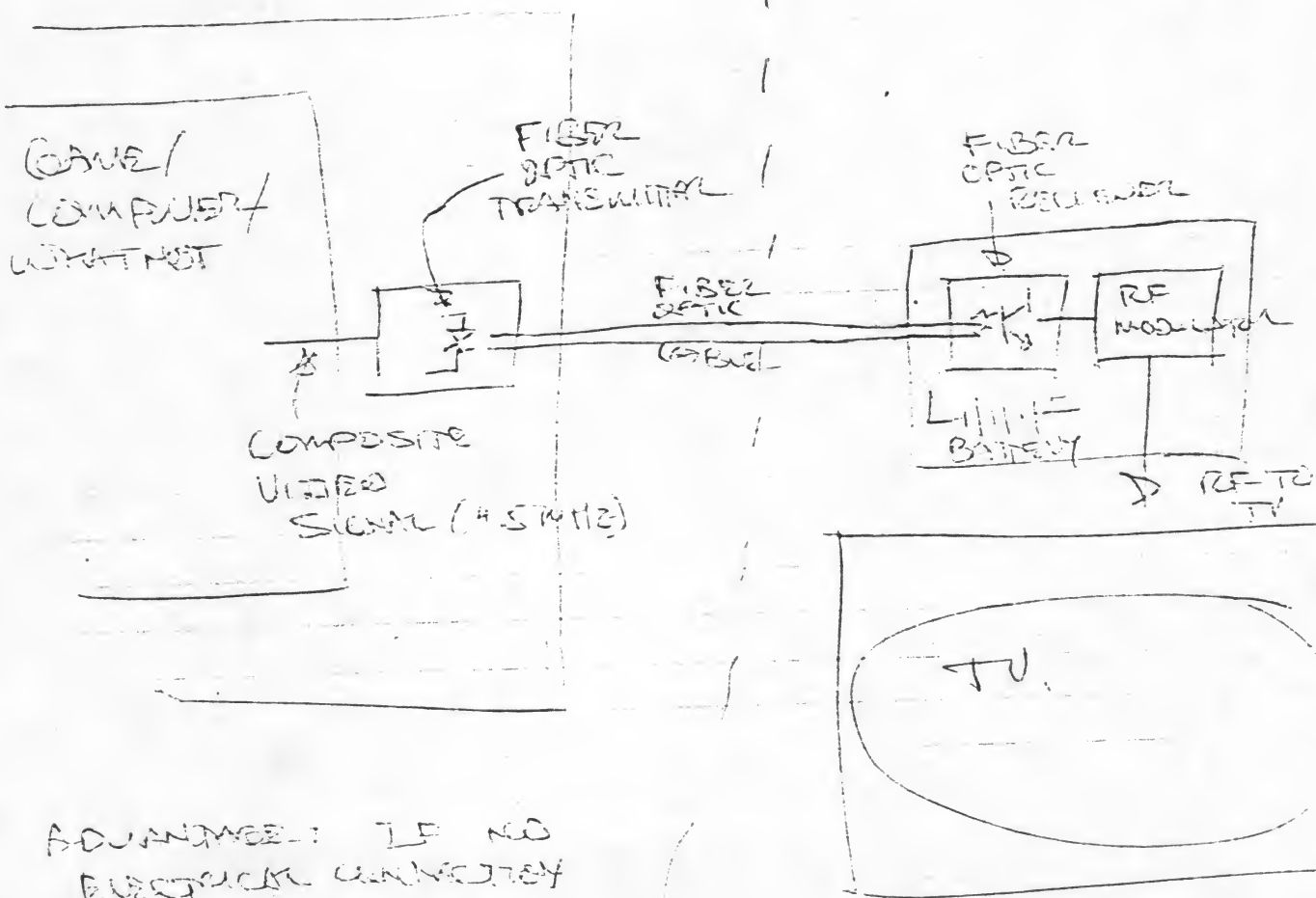
GAME OR PROJECT

GENESIS

HOT IDEA W/ MADE TUNA

METHOD FOR TRANSMITTING VIDEO TO

DEVELOPER TO USE WORKING ABOUT 100



BOUNDARY IF NO  
ELECTRICAL CONNECTION  
FROM GAME TO TV.  
PERHAPS GAME/COMPUTER  
DOES NOT HAVE TO PASS  
TYPE I APPROVAL.

0  
0  
0  
0

GAME OR PROJECT

STELLA COST PRODUCTION.

14 JULY. MOS TECHNOLOGY,

RAY HIRT.

JULES ~~HERTSCH~~  
HERTSCH.

WILL WATHMAS

8 AUG 77

~~COST ESTIMATE~~

CHIP SIZE ESTIMATES ON  
SEVERAL APPROACHES,  
DELIVERY DATES FOR SAMPLE & PRODUCTION.

MONTH  
DELAY FROM  
MOS TEST  
TO SYNTHESIS  
& PACKAGING

- 1) (6507 + PARTS OF 32)
- 2) (6507 + 1/4 TIMER) + 6810.
- 3) (6507) + (REDUCED 32)
- 4) (6507) + (REDUCED 32 w/ RAM) + 6810.

VS 5) 6507 + 6532 AS IS.

6) #5) - W/O TEST  
FURTHER DOWN ON LEARNING CURVE.

PARTS OF 32 WE USE:

PA, BIDIRECTION.

PB, BITS INPUT.

TIMER, 7, 8, +64

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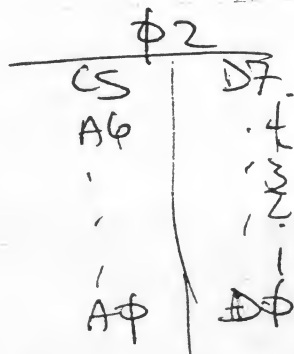
GAME OR PROJECT 6600
-------------------------

CAN BRING IN  $\phi 2$  (1.2 MHz)  
 IF YOU DON'T BRING OUT  
 ADDRESS MULTIPLEXED WITH DATA.

CAN BE BONDED (LAD OUT)

WITH.  $\frac{\phi 2}{CS}$   
 AS  
 .  
 $A\phi$ .  
 PAR STELA.

CAN BE BONDED.



**CONFIDENTIAL**

GAME OR PROJECT

6600

~~PROLOG~~

TAKES 1 DAY TO TWO WEEKS  
TO LAY OUT PERIPHERY.

MAX  
SPEED

MASK TURNAROUND IN 1 DAY - 1 WEEK

6-8 WEEKS FOR REASONABLE  
TURNAROUND.

TURNAROUND FOR DIFFERENT MASK.

IS THE SAME AS ANY  
PERIPHERY CHANGES.

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SAMPLES IN FEBRUARY

EMULATE IT

WITH 6522'S AND

6502, AND RAM AND ROM.

APPROXIMATE

32x8	512x8	200mil
64x8	1Kx8	
128x8	2Kx8	





GAME OR PROJECT  
6600

EXPANSION COMPATIBLE w/ 8048

SUGGESTED 8041 TYPE DEVICE

VERSION DESIGNED TO  
INTERFACE w/ VIC. COMING  
LATER.

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MCKENNEY,  
CHARPENTIER

CLOCKS ARE FIXED IN HORIZONTAL SIZE -  
BUT YOU CAN TURN OFF SOME OF THEM.

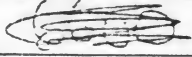
- PROBABLY GENERATES ADDRESSES OFF  
HORIZONTAL COUNTER,

CONFORMABLY - 23-24 CHARACTERS  
ADDRESS

1440  $\times$  240 lines  
577 WITHIN 8x8

14.3818  
- 2.5  
-----  
11.8818 = 4.0909.

GAME OR PROJECT



VIC.

CONFIDENTIAL

HORIZONTAL 258 CLOCKS

192 DOTS. EXAMINE

TURN OFF DISPLAY BY  
PUTTING IT OFF SCREEN.

NO INTERRUPTS FROM VIC -

~~AND~~ TURN OFF SCREEN w/TIMER.

~~CPU RUNS @ 14/3.5/4.~~

16 BYTES OF CONTROL

0,1 HORIZONTAL AND VERTICAL POSITION OF  
TOP LEFT OF DISPLAY w/RESPECT  
TO HSYNC

HSYNC  $\pm 81$  FROM

DOES  
INTERLACE,

~~2,1~~ 2,3, V.H. COUNTER SIZE COUNTER

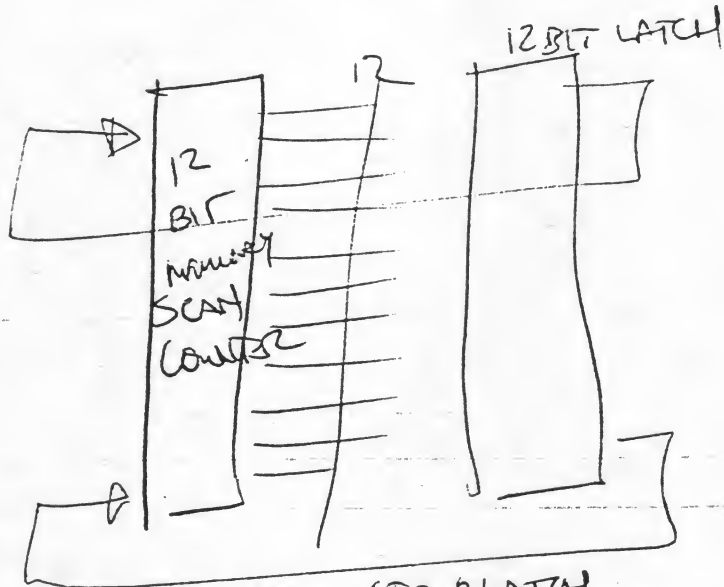


COMES OUT w/ COMPOSITE SYNC, COMPOSITE LUM,  
COMPOSITE COLOR.

GAME OR PROJECT  
VIC

ADDRESS COMPUTATION.

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CLEAR - CLR & LATCH.

COUNT UP.  
 JAM LOAD  
COUNT UP  
 JAM LOAD  
  
 COUNT UP. AND RELOAD LATCH  
 JAM LOAD  
 COUNT UP.

LINE OF CHARACTERS.

(no H or V reflect)

GAME OR PROJECT

VIC

2 POTS - 8 HORIZONTAL LINES PER CONVERSION 8 BITS.

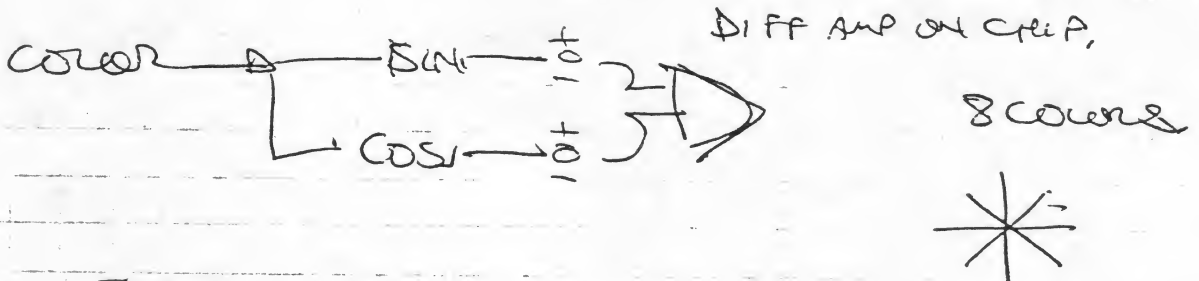
US CHIPS 4052B FOR EXPANSION.

~~REO~~ REO A, B, C, D, E SOUND.

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12 BIT WIDE MEMORY FOR COLOR.

QUADRATURE GENERATOR ON CHIP.



TWO GUNBE CHROMA.

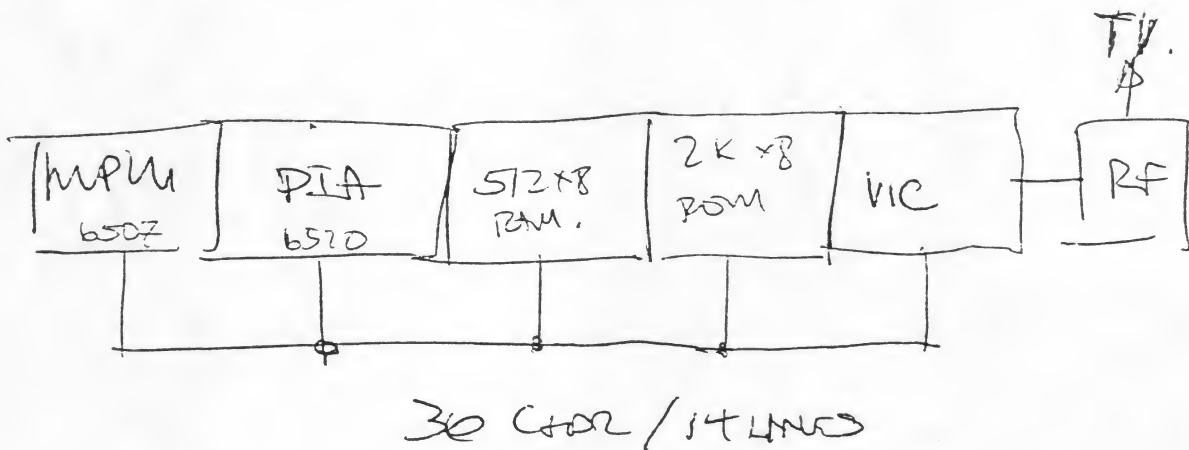
WHITE, BLACK & SIX COLORS

TWO GUNBE LUM.

AUDIO. 3 SINE GENERATORS (7 BIT DIVIDERS) + 1 16 BIT POLYNOMIAL CTR.

GAME OR PROJECT

ADDA



PERHAPS CHANGE VIC

TO RUN AT SLOWER CLOCK -

TURN OFF PROCESSOR

TO ALLOW DOUBLE

FREQUENCY ~~OF~~ CHARACTERS.

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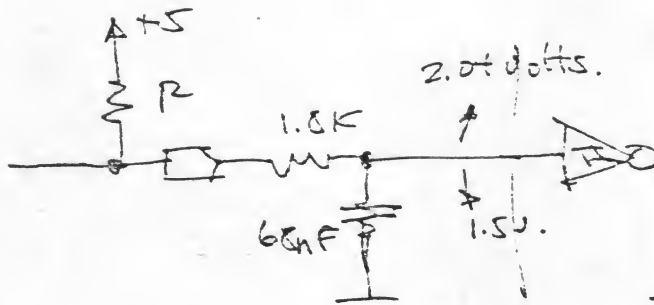
GAME OR PROJECT

KAY.

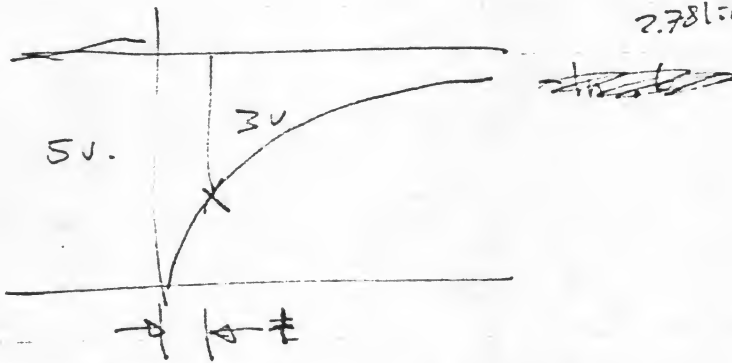
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CHOICE OF PULLUP RESISTOR

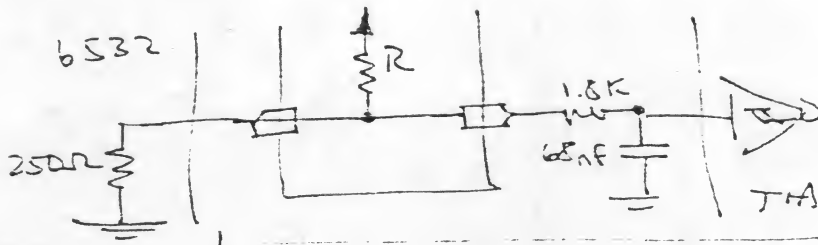
pulling up.



$$-RC \ln .6 = t = 410 \mu\text{sec.}$$
 if  $R = 10K$ .  
 $3.71 \mu\text{sec} = 236 \mu\text{sec @ } 5K$   
 $2.78 \mu\text{sec} = 177 \mu\text{sec @ } 3.3K$



pulling down.



$$RC!$$

$$R = 1.3K + 250R$$

$$1.328 \tau @ R = 5K$$

1.5V.

$$5 \times \frac{250}{250TR}$$



GAME OR PROJECT

KAY

$$250 \parallel 10K = 244 \Omega$$

$$244 + 1.8K =$$

$$250 \parallel 5K = 238 \Omega$$

$$\text{---} 2.044$$

$$250 \parallel 3.3K = 234 \Omega$$

$$R = 2K * 68nF = 136 \mu\text{sec.} = \tau$$

x x  
x x

$$\text{if } R = 5K \frac{250 + \cancel{5K}}{5.25K} * 5V = .238 \text{ volts.}$$

$$\Rightarrow 181 \mu\text{sec.} = 1.328 * 136 \mu\text{sec.}$$

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GAME OR PROJECT

PAL STELLA

EXPERIMENT

- 1) DISCONNECT AUDIO IN MODULATOR NETWORK FOR OLD KIM SYSTEM (MOUNTED ON BOARD)
- 2) TWEAK MODULATOR FOR 62.25 MHz.
- 3) CONNECT RF OUT TO GROUNDING TV-SET TO CHANNEL 3.
- 4) ADD ~~HORIZONTAL~~ LINES TO VERTICAL BLANK AREA IN COMBAT GAME CODE.  
314 LINES OF ~~THE~~ FRAME.

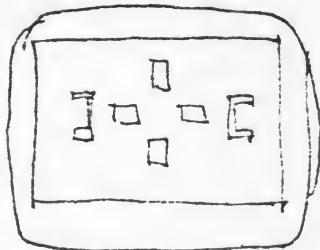
DERIVATION.

$$\frac{3579575 \text{ Hz}}{228} = 313.99517 \text{ LINES/FRAME}$$

50

LOOKS OK !!

TANK ASPECT RATIO OK.

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WRITER JSCUR

DATE 1-20-77

WITNESS

DATE

GAME OR PROJECT

PAL STELLA

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$$4.43361875 \text{ MHz} \times \frac{4}{5} = 3.5468949 \text{ MHz}$$

$$\div 228 = \frac{15,556.556 \text{ KHz.}}{15.6113} \approx 1.0035$$

5675 is spec.

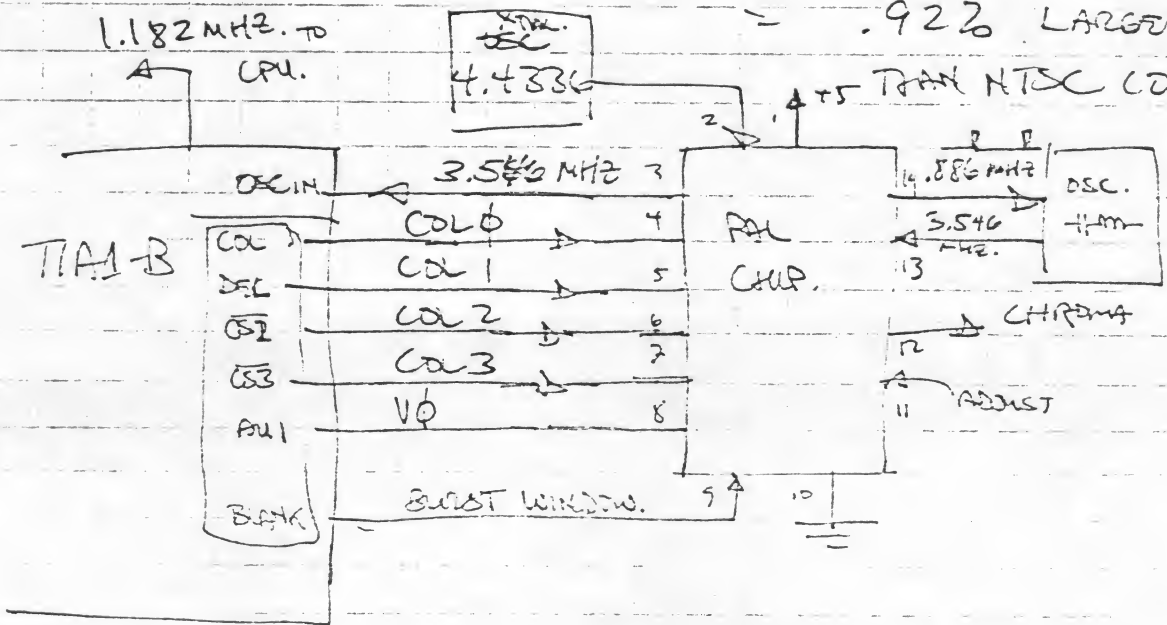
.3526 FREQ. M H

$$\frac{15556.556 \text{ Hz}}{50 \text{ Hz}} = 311.13113 \text{ LINES/FRAME.}$$

622 vs 625

$$\frac{3.5795454 \text{ MHz}}{3.5468949 \text{ MHz}} = 1.009205$$

1.182 MHz. TO CPU. = .922 LARGER.



JAY MINER

GAME OR PROJECT  
MOTOROLA 6809

FRANK MAHONEY      ST-500

SKIP STRUBER      SYSTEM DESIGN

JOEL BOVET      SYSTEM DESIGN

BOB NOSID      PLANNING

DISEWIRE:

3 temp range  
3 speed ranges  
mil FP3

HIERARCHY:

Save Facet: new peripherals  
new memory support  
new memory  
new interface

1,2 chip minime systems 6801; 6802+6846  
high performance upgrade of 6800

2ND QTR 78

MTI up for renewal in Oct '77

Source ~~comp~~ compatible - but not object compatible

95% DESIGNED - commit spec at end of 3/6/77

INTRODUCE 3RD QTR 78

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GAME OR PROJECT

WOTOPOLA 6502

5V CHIP CLOCK. 5V, BUS COMPATIBLE

8 BIT WORD SIZE 16 BIT ADDRESS

2MHz MINIMUM CLOCK

TARGET 20mil

NO illegal opcode

Memory RDT.

INSTRUCTION SYNC

BUS REQUEST, BUS GRANT

FAST IRQ (JUST PC AND STATUS)

PERHAPS

HAVE TRUE CLOCKS.

PLEASE ADD AT LEAST ONE ACCUMULATOR

IRQ ACKNOWLEDGE - VECTOR SELECT

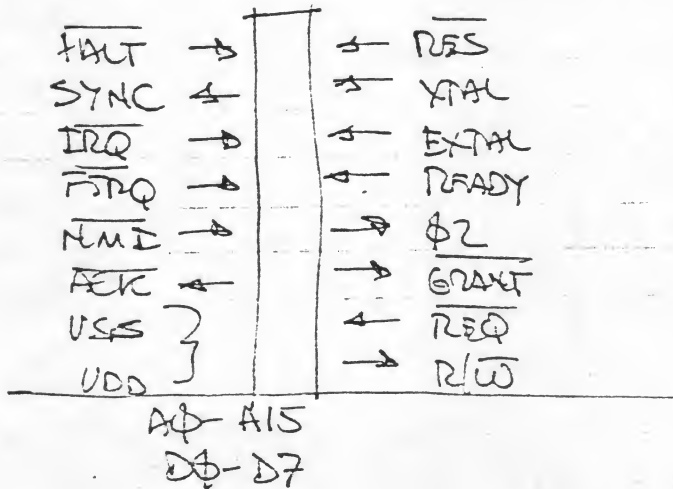
IRQ MAY BE VECTORED BY DEVICE

"2MHz"

requires 225nsec accesses.

- Increase size of address drives to save cost of memory.

TWO  
IRQ  
PINS.



Keep data, address, φ2, R/W for analysis.

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GAME OR PROJECT  
 MASTERPIECE 6800

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TWO ACCUMULATORS  
 TWO INDEX REGISTER  
 TWO STACK POINTERS - 1 AS IN  
 FIRST BUS ARCHITECTURE  
 DIRECT PAGE POINTER

16 BIT WIDE

not doing low byte - high byte  
 chip designer wanted to do it  
 not source compatible

upward source compatible.  
 80 instructions consistent mnemonics.

16-32  
 byte  
 opcodes.

348 op codes  
 8x8 multiply unsigned A+B → A,B / mostly for  
 16 bit operations index calculation.  
 bit manipulation or memory  
 powerful stack instructions  
 register transfer & exchanges.

ADDRESSING MODES

11 ADDRESSING MODES

200 of  
 instructions  
 - 16

DIRECT VIA PAGE POINTER  
 INDIRECT ADDRESSING ADDED TO INDEXED MODES.  
 UP TO 16 BIT SIGNED INDEXED OFFSET.  
 AUTO INCREMENT / DECREMENT  
 ACCUMULATOR INDEXING. A+X →

A, B + 2 BYTES IN MEMORY.

FIX CONSTRAINTS ON INX, DEY →  
 create add immediate to index registers.



GAME OR PROJECT

INTERPOLAR 5759

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SOFTWARE DESCRIPTION

- POSITION INDEPENDENT CODE (16 BIT BRANCH ADDRESS)
- NON SELF-MODIFYING CODE
- STRUCTURED, HIGHLY SUBROUTINED CODE
- MULTITASKING AND MULTIPROCESSING
- STACK ORIENTED COMPLEX INSTRUCTIONS
- OPERATING SYSTEM CALLS - 3000 INSTRUCTIONS
  - 3 2-BIT CALLS } 2 BIT CALLS = 3
  - VERTICALS } 1 16 BIT CALL = 1

RFS, LTR, FIRQ, NMI, SWI,  
OSC 1, OSC 2, OSC 3.

8 BIT

DIRECT PAGE PTR	COND. CODE REG.
A	B
	IX
	IY
	US
	SP
	PC

DECREMENT & BRANCH NOT EQUAL INSTRUCTIONS.

LOAD MEMORY IMMEDIATE

ADDRESSING MODE:

DATA.

IMPLIED

IMMEDIATE

DIRECT

RESTRICTED (ABS)

INDEXED

: IMMEDIATE OFFSET

• REGISTER OFFSET

INDIRECT OFFSET

" AUTO INCREMENT

" AUTO DECREMENT

ALSO LONG BRANCH

GAME OR PROJECT

P. ETTER... 1979

THERE EXISTS A  
 DOUBLE LENGTH MEMORY INCREMENT  
 AND BRANCH  
 AND 2 BIT LENGTH

## 16 BIT INSTRUCTIONS.

DOUBLE ADD  
 " LOAD  
 " STORE  
 " COMPARE  
 " SUBTRACT  
 INCREMENT, ~~INCREMENT~~ MEMORY  
 NO BRANCH NOT EQUAL  
 SIGN EXTEND. SET MEMORY

## BIT MANIPULATION

- BIT SET - w/ memory
- BIT CLEAR - ~~ADD~~  $\rightarrow$
- BIT TEST
- TEST & SET
- BIT TONE - for w/ memory.

## RELATIVE INSTR.

- LOAD FROM RELATIVE
- LONG BRANCH TO SUBROUTINE
- LONG BRANCH &

PPH  
 3 2 1 0

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DATE

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DATE



GAME OR PROJECT

METEOR

THAT EXISTS A  
 DOUBLE LENGTH INSTRUCTION  
 AND BRANCH  
 AND 2 BIT LENGTH

16 BIT INSTRUCTIONS.

DOUBLE ADD  
 " LOAD  
 STORE  
 COMPARE  
 SUBTRACT  
 DECREMENT, ~~INCREMENT~~ MEMORY  
 NO BRANCH NOT DONE  
 SIGN EXTEND. SET MEMORY

BIT MANIPULATION

- BIT SET - w/ memory
- BIT CLEAR - ~~AND~~ →
- BIT TEST
- TEST & SET
- BIT TOGGLE - for w/ memory.

RELATIVE INSTR.

- LOAD ADDRESS RELATIVE
- LONG BRANCH TO SUBROUTINE
- LONG BRANCH #

??!!  
 3 3 3

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WRITER

10/1/73

DATE

WITNESS

DATE

GAME OR PROJECT

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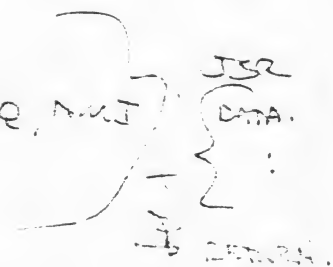
## PULL AND PUSH

- PULL FROM REGISTER
- PULL FROM ADDRESS REGISTER
- PULL FROM I/O
- PULL FROM I/O
- INCREMENT FROM REGISTER AND I/O
- PUSH TO REGISTER AND I/O

## SUBROUTINES & INTERRUPTS

- RETURN USING ADDRESS
  - RETURN FROM FAST I/O
  - STOP → CALL IT SYNC
  - OPERATING SYSTEM CALLS (?)
  - SOFTWARE EXECUTION OF I/O, P.I/O, N.I/O
- (STILL HAVE WAIT FOR INTERRUPT)

2 PASSING OF DATA IN CODE



## SOFTWARE RESET

SHOULD RESET WHOLE SYSTEM.

## REGISTER

- TRANSFER REGISTER TO REGISTER
- EXCHANGE AND REGISTER
- ADD TO X, Y, U, or S immediate
- ADD A TO X, Y, U or S
- LOAD, STORE, ST, P.O.R., AND COMPARISON CODES
- LOAD STORE A, B, X, Y, U, S, CCR, D, DP
- COMPARE X, Y, U, S, AND Z

## MISCELLANEOUS

- BPS → 16      A & B → B, A
- DECIMAL & BINARY NOT COVERED
- DECIMAL ADD A & B
- INCREMENT SUBTRACT A & B
- MORE TO BE DONE TO MEMORY.

GAME OR PROJECT

MILITARY

ELECTRIC BUILDING

A 220V 3PHASE EQUIPMENT  
TO PLUG INTO EXERCISE.

2 220V'S + MICROCASE

QUESTIONS ABOUT HIGH LEVEL  
LANGUAGE

TOM ADDIE

TEXAS INSTRUMENTS

DM 1048 FIBER OPTIC JUNCTION / RCVR 10FT LINK

\$175 BOOK DEPARTMENT A20

776 PALOMAR

SUNNYVALE, CA 94086

732-1840

est. MID 1976:

# 100K	6.55
250K	4.88
500K	3.90
2M	3.75

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WRITER JOE DEQUER

DATE

WITNESS

DATE

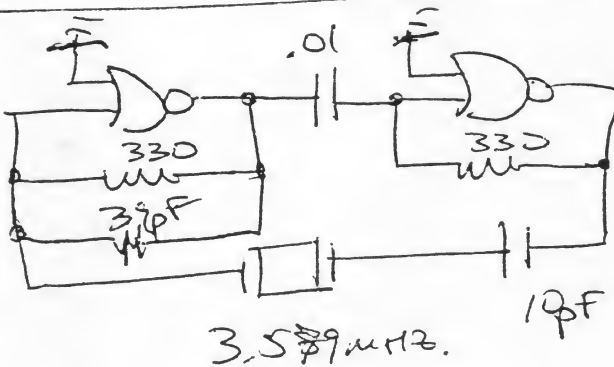
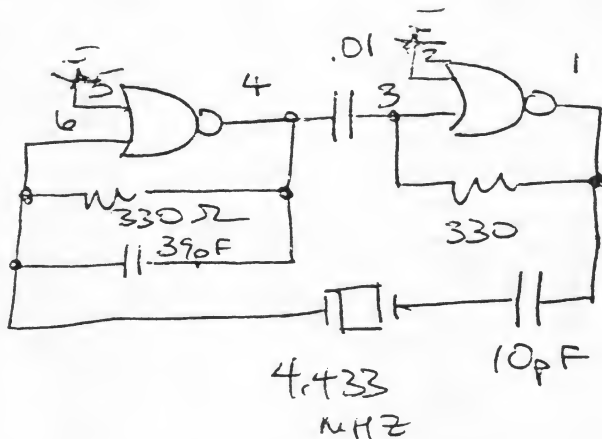
GAME OR PROJECT

PAL STELLA

TEST CIRCUIT FOR JAY'S

LOCKED OSCILLATORS DATA:

OSCILLATORS:



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GAME OR PROJECT

TANIGAS Instructional

0077

they will develop 2 new  
members of 9900 series,  
which will be specific to  
particular market segments

get our opinions on things  
that are useful for us.

they are 2nd sourced w/ AMI

review of 9900 ARCHITECTURE.

LOOK INTO CPU DETAILS.

I/O IS CPU of memory mapped.

ADDRESSING MODES

WORKSPACE REGISTER  
DIRECT REGISTER  
INDIRECT WITH AUTO INCREMENT  
INDEX immediate register  
SYMBOLIC (DIRECT)  
IMMEDIATE  
PC RELATIVE (JUMP)

WRITER D.E. BEOUR

DATE 1/27/77

WITNESS

DATE

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GAME OR PROJECT

TMS 9900

ALL

PROGRAM CONTROL

MOVES

LOGICAL

SHIFTS     a bit shifts

I/O     (CRU CONTROL)

RETURN

3 MHz clock     500 ns memory

BROWSEM     2.67

ADD     4.67     R-R

MPLY.     17 μsec.     16 × 16

DIV.     41 μsec.     16 × 16 !!

MOV     7.33     reg to direct X

**CONFIDENTIAL**

**CONFIDENTIAL**

GAME OR PROJECT

TI 9940

SBP 9900

I<sup>2</sup>L

9900

TMS 9930

MULTIPLEX DATA BUS.  
14 ADDRESS LINES.  
ON CHIP CLOCK !!

TMS 9940

SAMPLES 1ST QTR '78

128 BYTES RAM  
2K ROM ON CHIP w EPROM  
4 INTERRUPTS IN  
16 BITS OF CPU.

32 GENERAL I/O LINES

75V.

25K BITS EXTERNAL.

POWER DOWN MODE

5MHz operation

clock oscillator on chip

14 BIT ~~3~~ TIMER

PIPELINED 8 BIT MACHINE INFINITELY.

See  
9940  
writeup.

8 YOP'S - SOFTWARE INTERRUPTS.

MULTIPROCESSORS INTERFACES

- serial port from to  
another device bit rate  
{25-30 kbaud} 2.5 MHz.

Separate power for ram, flags, r, inter.  
and for everything else

CONFIDENTIAL



GAME OR PROJECT

T199 #10

est (200 mil)<sup>2</sup>

est \$10 price  
"design goal"

good controller  
poor memory expansion.

Kevin McDonough,

Drums,  
MS FET (IEEE 50-10)  
STATE

new processors

99XX 64 PIN PLASTIC PACKAGE

~~SP~~ MULTIPROCESSING  
EXTENDING ADDRESS SPACE (separate  
memory management)

MICROPROGRAMMED ARCHITECTURE

⇒ FLEXIBLE INSTRUCTION SET.

9900 base set

base enhancement (signed multiply & div)

99E0 ADDITIONS

BYTE STRING OPERATIONS

STACK OPERATIONS

BIT & FIELD OPERATIONS

MULTIPLICITY & INT. RES.

DECIMAL OPERATIONS

CONTROL

FLOATING POINT

CONFIDENTIAL



GAME OR PROJECT

~~TRIS 9903~~ ANTIC

REVISIONS IN ANTIC.

ALL MODES LOAD THE SHIFT REGISTER  
ON THE FIRST

FIX . . .

MAJOR CONCEPT, w/ STAFF  
CONSENSUS.

TWO PACKAGES.

BASIC BOX WITH CPU,  
4K BYTES RAM,  
TAPE  
ANTIC  
STELLA X  
488 and/or RS232  
GAME CONTROLLERS,

I PLUG IN ROM  
SOCKET FOR: e) BASIC  
b) SUPER GAMES  
c) PHONE CONTROL  
d) ~~TRIS~~ - EDUCATION  
PACKAGE

**CONFIDENTIAL**

WRITER

DE CUIR

DATE

9/1/80

WITNESS

DATE



GAME OR PROJECT

COLORET,

ASIDE) ATARI SHOULD  
START WITHIN 45  
SMART TELEPHONE

PERHAPS, DELETE T88  
AND DEFINE A SERIAL  
BUS - BECAUSE  
NOTHING NEEDS THE SPEED  
EXCEPT THE DISK.

STUDY CPU CONCEPT OF  
9900 SOME MORE.

FOR USE  
VIA

⇒ POKET HAS POTS  
KEYS  
SERIAL BUS

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DATE

GAME OR PROJECT  
CONFIDENTIAL

MINIMUM BOX, LSI - COSTS 80-90% OF MARKET

- 5 CPU (6809, 6509...?)
- 10 6-8K BYTES OF ROM
- 16 4K BYTE RAM, PROGRAM, WORKING STATE, SCORE MAP.
- 4 PIA(S) TAPE CONTROL GAME CONTROLLER PANEL SWITCHES.
- 6 ANTIC TV ~~CONTROL~~ NON MOVING VIDEO.
- 4.50 TH-2 OBJECT GENERATION, AUDIO
- 4.50 POKEY KBD, POTS, SERIAL I/O EXPANSION, LIGHT PEN.
- ~~4.50~~ LSI.
- 50

- PLAYS: STEVE TYPE GAMES - (4 PLAYER)
- : DRESSET SOFTWARE
- : SIMPLE BASIC
- : PROGRAM SOME GAMES.
- : COMPATIBLE WITH ~~SOME~~ SLOW I/O DEVICES: TELEPHONE HOUSE MUSIC/SPEECH BURGALAR ALARM. ZNO TAPE.

CONFIDENTIAL

2ND BOX - PLUGS INTO #1.

- BUS EXPANDERS,
- BIG POWER SUPPLY.
- 1 OR 2 SLOW PERIPHERALS.
- 488 BUS.
- RESIDENT DOS ROM.
- ~~SOME FOR RAM & ROM~~ 8K BYTES OF ROM
- NO PUSHS

GAME OR PROJECT

COLSON

2ND BOX.

COSTS

\$ 32	8K RAM.
0	4K RAM. DOS, BOOTSTRAP, ETC.
8	68458 + DRIVERS.
6	DISK CONTROL.
	( <del>DISK CONTROL</del> or SDC + P/A)
<u>\$ 48</u>	(DISK CONTROL)

+ TWO SLOW DISK DRIVES.

HARDCOPY - USE DAISY WHEEL

OR SOME OTHER IMPACT  
PRINTER -

PERHAPS BUY - OEM.

THE CARTRIDGE & PLATEN & RIBBON  
ASSEMBLY FROM A SCM  
TYPEWRITER (BITS OF  
ELECTRIC TYPEWRITER)

ADD SMALL SCANNER (IN A DOT  
MATRIX PRINTER) AND FACSIMILE  
TRANSMISSION BEHINDS POSSIBLE.

**CONFIDENTIAL**

GAME OR PROJECT

CONFIDENTIAL SYSTEM.

WRITE PROPOSAL IN ENGLISH.

MARKETS: CAR PLAYER  
 SMALL BUSINESSES  
 TECHNICAL PEOPLE MARKET

CONSIDER USING

82S23 or 82S123

32+8 BIPOLAR PROM

PROBLEMS ASSOCIATED WITH

PROXY - REQUIRES 4 BITS/POINT

AND EXTRA DMA CYCLES, OR

PARALLEL RAM.

**CONFIDENTIAL**

WRITER

J. E. DREW

DATE

1/16/76

WITNESS

DATE

GAME OR PROJECT

Colleen

~~POSSIBLE~~ POSSIBLE  
MEMORY MAP:

4xφ	MAINFRAME RAM
1	
2	ADD ON RAM
3	
4	more ram?
5	
6	I/O
7	
8	PLUG IN ROM SPACE
9	(EXTENDED BASIC, or BUSINESS,
A	or EXTENDED GROSS, or PHENIX
B	or HOUSE CONTROL/CONTROL, or COMPLEX)
C	DISK MACHINE OS
D	AND HANDLES.
E	MAINFRAME MONITOR, INTEGER BASIC, TAPE HANDLER.
F	SERIAL HANDLER, CONTROL SET

MAINFRAME  
4K RAM  
8K RAM  
PIA  
TIA2  
ANTIC  
POREY

ADD ON  
8K RAM (16K)  
4K RAM (8K)  
DISK I/O  
G.P.A  
RS232

ANTIC SCREEN MGR, RAM REST  
TIA2 MOVING OBJECTS, HULLD  
POREY POTS, KEYBOARD, SERIAL  
PIA(S) TAPE, PANEL, CONTROLLER  
} PIA DISK I/O } DISK CONTROL  
} SEDA }  
G.P.A. IEEE 488  
G.C.A. RS232

(ADD MEMORY  
PROTECT VIA PIA'S)

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WRITER JES DEWILL

DATE

WITNESS

DATE

GAME OR PROJECT

ANTIC.

## THINGS TO DO ON RETURN.

1. PUT ANTIC ON CUSHY  
MEDIUM AND TRY  
OUT ON TV TO VARY  
ASPECT RATIOS OF GRAPHICS,  
CHARACTERS, RESOLUTION OF  
20, AND 40 CHARACTER OBJECTS,  
EXAMINE EFFECTS OF COLOR  
40 CHARACTER (140use dot)  
GRAPHICS. - ON COLOR TV,

Dr. Mincucci  
956-3420

MOVED TO  
22ND  
9AM.

meeting of 9th

JAY  
FELS  
ALCOHOL  
BROWN  
LUNCH.

ACCEPTED JAY'S CONCEPT  
OF MAINFRAME: TAPE

ANTIC & TIA

D.A. & POKER

CPM

4-8K OS ROM

4K ROM

EXPANSION BOX w/ CARD SLOTS

FOR ROM

EXTENDED BASIC

ETC.

SIGNAL COMPATIBILITY NOT REQUIRED.

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WRITER

J. Mincucci

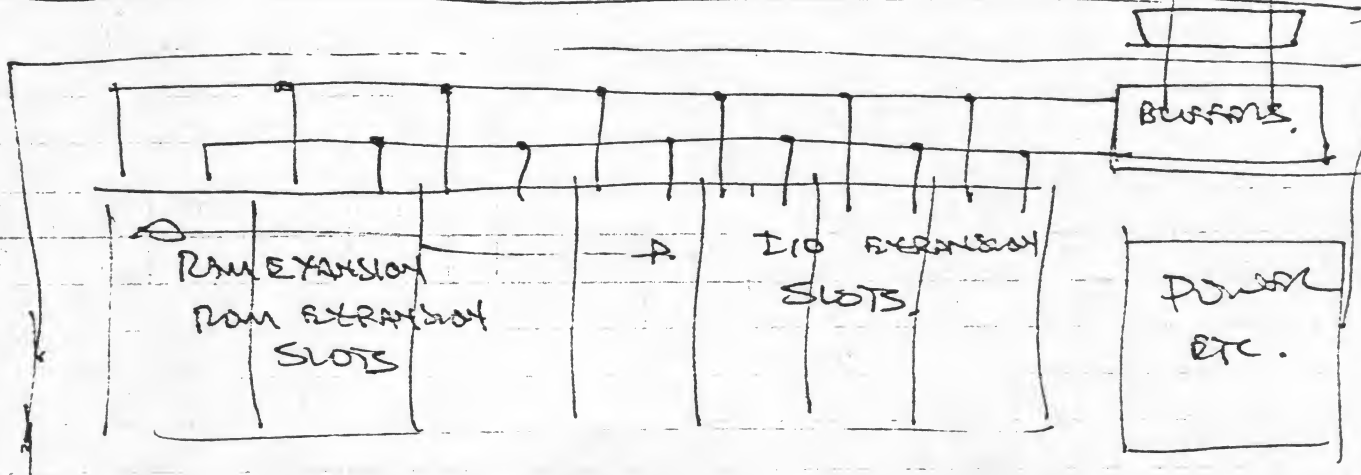
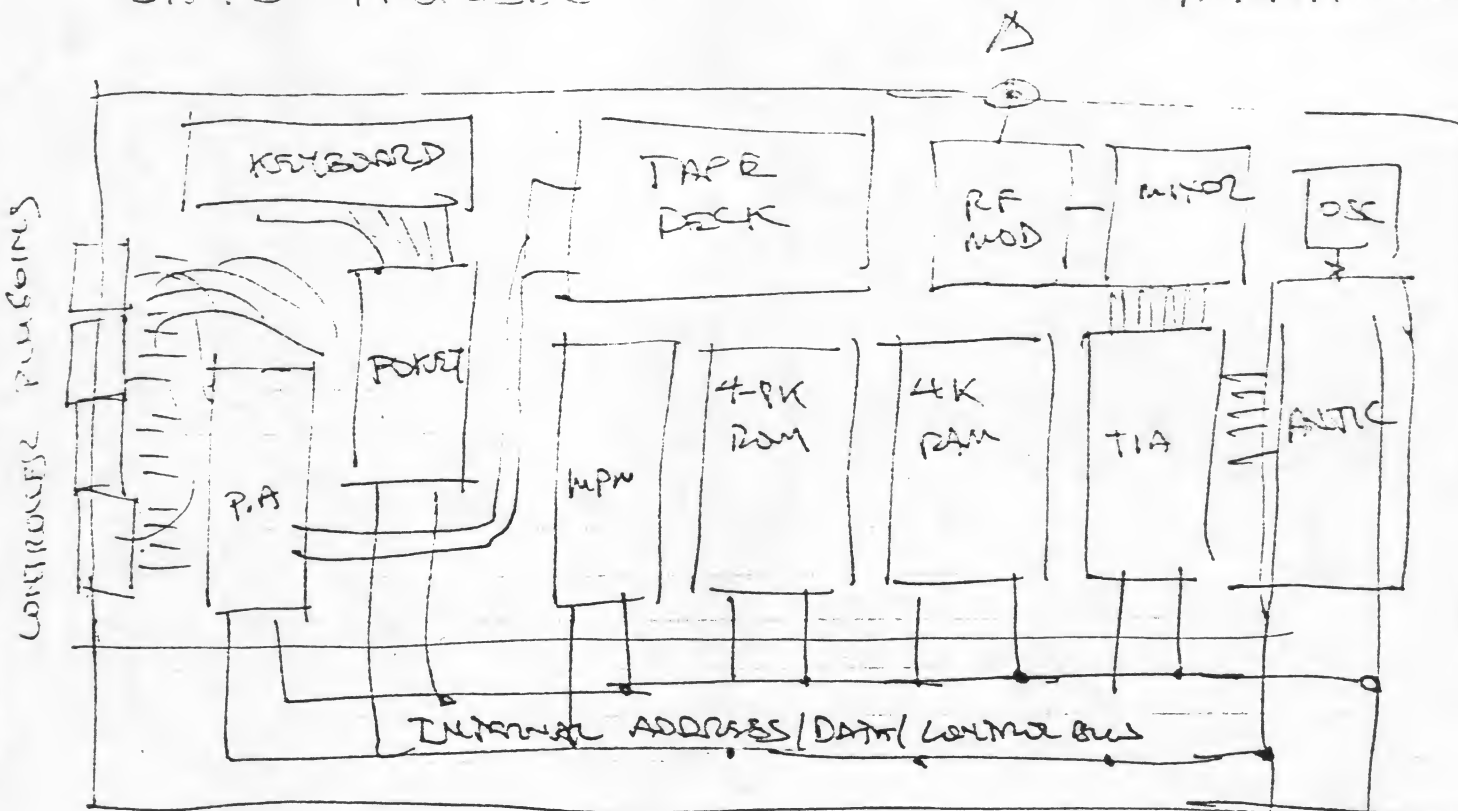
DATE

WITNESS

DATE

JAY'S PROPOSAL

MAINFRAME



ADD ON

BASICALLY ACCORDS  
BY BROWN, ALCOBY, FULLS, WHICH

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GAME OR PROJECT

COLECO

STEVE WANTS TO SEE CAPABILITY

BETTER TO BUILD THINGS IN IF  
IT'S CHEAP -

KEEP TOTAL NUMBER OF  
DIFFERENT COMPONENTS DOWN.

DON'T NICKLE AND DIME THEM TO DEATH

DIFFERENCES:

- 1) ADD ~~2~~ SERIAL I/O EXPANSION  
AND SINGLE CARTRIDGE EXPANSION
- 2) 2ND UNIT IS SINGLE PACKAGE  
W/DUAL FLOPPYS, RAM, ROM, AND  
488 TYPE ~~8~~ I/O - RATHER  
THAN AN UNUSUAL MOTHERBOARD  
EXPANSION BOX

OUTLINE OF PROPOSAL

- 1) MAINFRAME IS ENTERTAINMENT MACHINE  
VIDEO GAMES  
DARTS  
PHONE  
HOUSE CONTROL  
MUSIC  
SIMPLE PROGRAMMING.  
DARTS TERMINAL

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GAME OR PROJECT  
COLLECT

2) 2ND MACHINE IS FOR  
SERIOUS WORK.

~~BE~~ DUAL DISKS, RAM & ROM,  
TO SUPPORT SERIOUS PROGRAMS &  
SOPHISTICATED PERIPHERALS.

COMPILES

SMALL BUSINESS DP

WORD PROCESSING

SCIENTIFIC NUMBER CRUNCHING

(SIMULATION, COMPUTER AIDED DESIGN,  
STATISTICAL ANALYSIS)

LOCAL PROCESSING FOR

~~SMALL~~ LARGE COMPUTER.

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STUFF TO BRING UP: VDAO MODULATOR?

COLOR TV.

COUPLE PROPERTY  
LISTINGS

PICKED UP AT P&O AUTO AIRPORT  
SUNDAY NIGHT

STEVE'S FOLKS  
415-368-8876  
TODD NEEDS CASH.

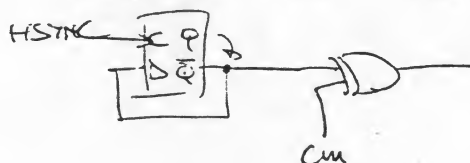
GAME OR PROJECT

PAL STELLA

GET PAL COLOR WORKING!!

THINGS THAT HELPED:

- 1) TUNE PAL COLOR OSCILLATOR TO 4.433613 MHz.
- 2) PUT RF AMPLIFIER ON VIDEO OUTPUT
- 3) FINER TUNING OF TV.
- 4) CHANGING POLARITY OF FLIP FLOP OUTPUT FOR PHASE ALTERNATION



- 5) ADJUSTING DELAY LINE PROPER DELAY CAREFULLY.

RUNNING WITH HSYNC =

$$228 \times \frac{5}{4} \times \frac{1}{4.433613 \text{ MHz}}$$

NO RGB EFFECTS NOTICED

ONE TARGET OR ONE MISSILES.

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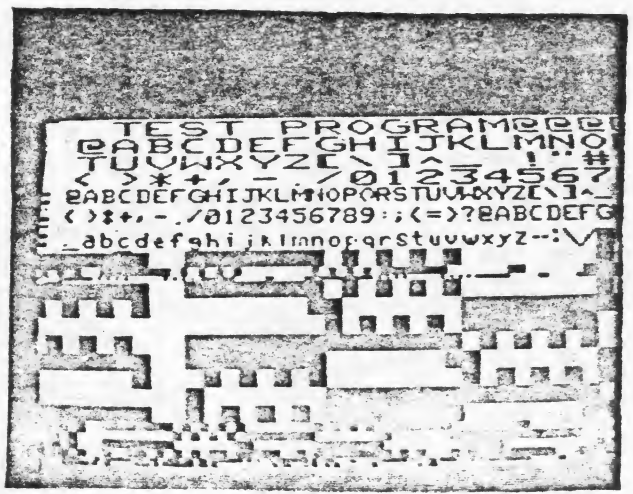
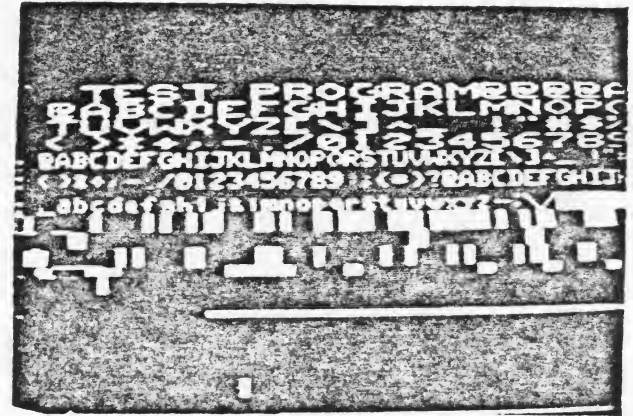
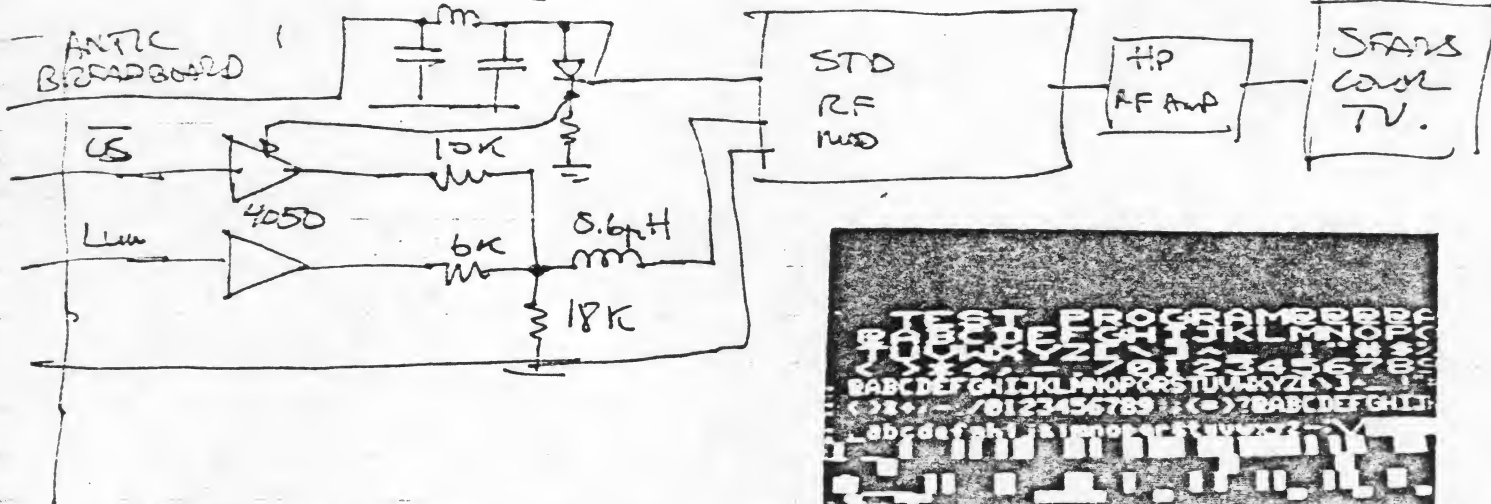
GAME OR PROJECT

ANTIC.

AUGUST 15, 16, 17, 18. WORKED ON ANTIC IN CLASS VALLEY.

MONDAY: INSTALLED RF MODULATOR

PUT 40 CHAR/LINE ON SCREEN. IN BLACK AND WHITE, ON A STARS COLOR TV (15"?)



~~RED~~ VIDEO SUMMING,  
RF INTERFERENCE ISOLATION,

AND RF AMPLIFICATIONS IS

BASICALLY IDENTICAL TO

STELLA, w/ TWO EXCEPTIONS:

- 1) NO COLOR BURST.
- 2) RF AMP USED TO ~~REDUCE~~ <sup>REDUCE</sup> ~~NOISE FROM~~ <sup>INTERFERENCE</sup> FROM BREAD BOARD AND PPP-11 COMPUTER NEARBY.

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GAME OR PROJECT

ANTIC BREADBOARD

CONFIDENTIAL

~~CONFIDENTIAL~~

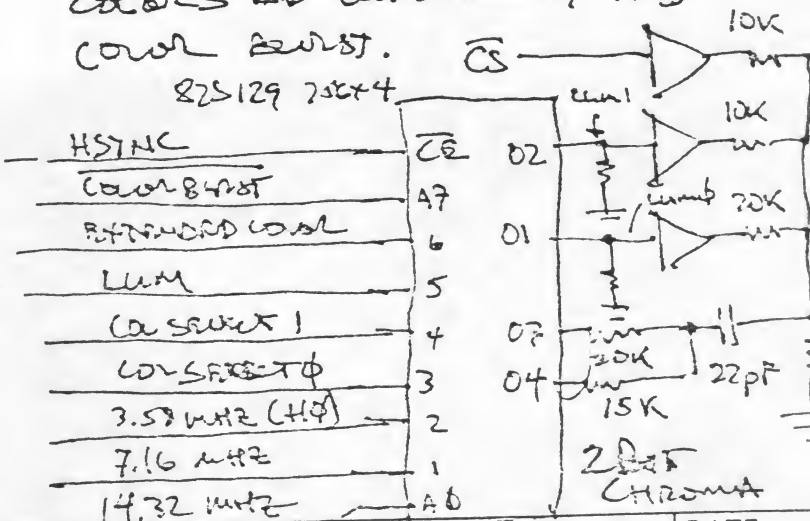
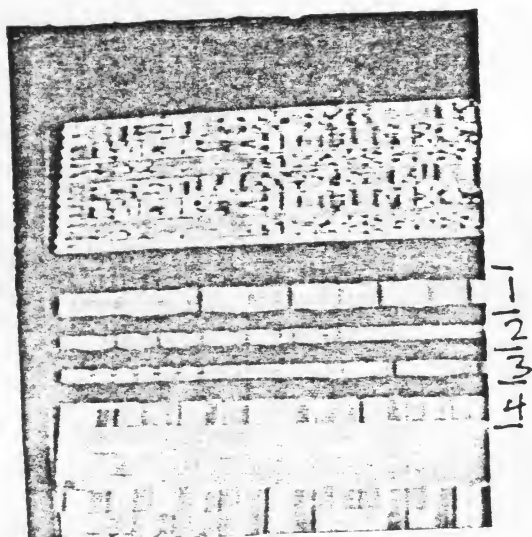
COMMENTS: AS CAN BE SEEN FROM POLAROID (SX-70) PHOTOS ON PREVIOUS PAGE, CHARACTERS ARE SHARP IN BLACK AND WHITE. DEPENDING ON CONTRAST, SOMETIMAS BLACK IS WHITE LOOKED SHARPER THAN WHITE OR BLACK.

SHARPEST CHARACTERS ARE 40 (8x8) / LINE.  
 DOT CLOCK = 2x NTSC COLOR = 7.16 MHz.  
 (LOWER BURST NOT SH!)

TUESDAY 16 AUGUST

ADDED COLOR USING 14MHz AND

SUB HARMONICS TO GENERATE COLOR WITH A PROM. OTHER INPUTS WERE USED TO SELECT COLORS AND LUMINANCES, AND COLOR BURST.



GAME OR PROJECT

ANTIC BROADCAST.

AS CAN BE SEEN IN THE ~~PHOTO~~ PHOTO,  
 COLORS WORK. IN THE HORIZONTAL  
 BANDS 1, 2, 3, 4. ~~THE~~ SCREEN MAP WORDS ARE  
 TESTED.

BAND 1 IS THE 40 BIT MODE:  
 10 DMA'S / LINE  $\Rightarrow 5 \times 8 \times 2 = 40 \times 2$  BITS  
~~40~~ 40 POINTS, 4 COLOR CLOCKS  $\times$  8 LINES  
 $\times$  4 COLORS. (STELLA AF RESOLUTION)

BAND 2 IS THE 80 POINT MODE:  
 20 DMA'S / LINE  $\Rightarrow 10 \times 80 \times 2 = 80 \times 2$  BITS.  
 EACH POINT 2 COLOR CLOCKS  $\times$  4 COLORS  $\times$  4 LINES  
 (APPROXIMATELY PARCHELLS RESOLUTION)

BAND 3 IS 3 REPETITIONS OF THE 160 POINT MODE:  
 40 DMA'S / LINE  $\Rightarrow 20 \times 80 \times 2 = 160 \times 2$  BITS.  
 EACH POINT 1 CLOCK  $\times$  2 LINES  $\times$  4 COLORS  
 (STELLA OBJECT RESOLUTION)

BAND 4 SAME AS BAND 1.

AT THE TOP OF SCREEN, 20 AND 40 CHARACTER  
 LINES ARE DISPLAYED W/ COLORS. NOTE THAT  
 THE CHROMA CARRIER MIXES WITH THE LUMINANCE  
 WITH PECULIAR RESULTS. THIS BRINGS  
 FURTHER STUDY (WHAT IF COLOR BURST  
 WATS ON, BUT NO COLOR CARRIER  
 DURING THE LINE?)

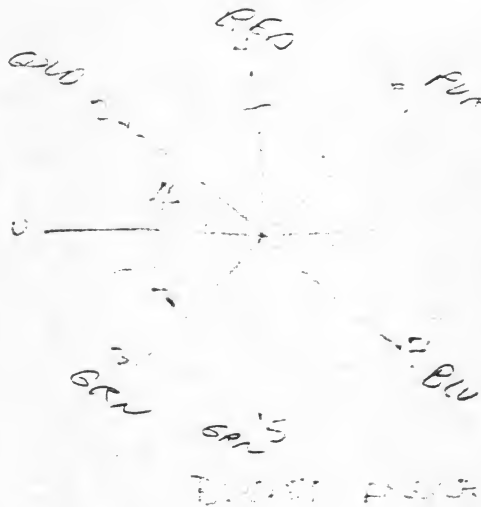
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GAME OR PROJECT

CRASH

CONFIDENTIAL

VERY BEACH NINE ...  
... PAL ...  
... FRAME



... 2.7 ...

BURST ... 20 usec ...  
color drops out ...

... 2.09 ...  
BURST ... = 20 usec ...  
color drops out.

... 90° = ...  
... = ...

$$\frac{9.9 + 7.4}{2} = 17.3 = 8.65$$

sensitivity of frequency

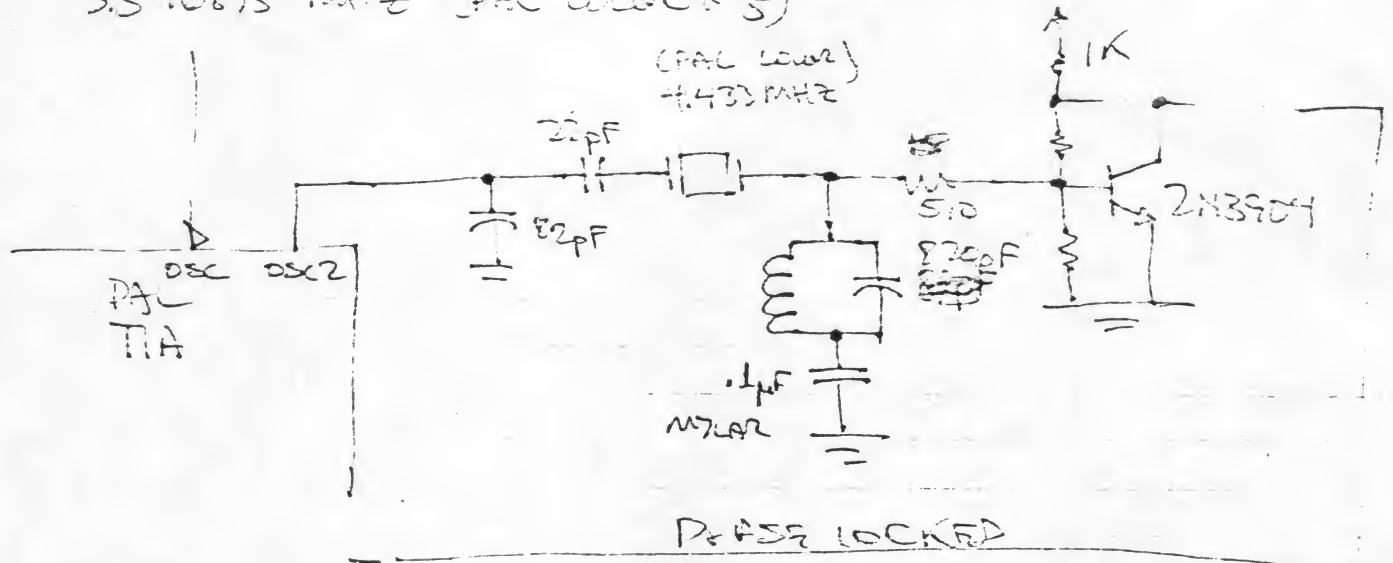
color momentary #43361075

Drops out ... 4,433,700 ...  
... 4,433,175

GAME OR PROJECT  
 SYNTHIA

NILES' CKT FOR PAL COLOR.

3.546895 MHz (PAL color  $\times \frac{4}{5}$ )



PHASE LOCKED  
 PAL COLOR 4.43361873 MHz.

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GAME OR PROJECT

ANTIC

EXTENDED COLOR

①

1

MODE

000

 BLANK- ~~XXXXXXXXXX~~  
 (1-8 LINES)

SPACE

001

 20 CHAR/LINE  
 2 COLOR BITS X 8 BITSUM.  
 2<sup>nd</sup> CHAR + 2 COLOR BITS,  
 8 LINES X 8 CHAR.

 20 CHAR/LINE  
 2 COLOR BITS / PAINT,  
 2<sup>nd</sup> CHAR + 2 COLOR BITS  
 (40 DWA/LINE)

010

 40 CHAR/LINE  
 2<sup>nd</sup> CHAR + INVERT COLOR  
 10 LINES X 4 COLORS (40 DWA/LINE)

SPACE

011

SPACE

SPACE

100

SPACE

SPACE

101

 MEM MAP  
 40 BITS/LINE  
 X 8 LINES  
 (5 DWA/LINE)

 MEM MAP,  
 40 X 2 BITS/LINE  
 X 8 LINES  
 (10 DWA/LINE)

110

 MEM MAP  
 80 BITS/LINE  
 X 4 LINES  
 (10 DWA/LINE)

 MEM MAP  
 80 X 2 BITS/LINE  
 X 4 LINES  
 (20 DWA/LINE)

111

 MEM MAP  
 160 BITS/LINE  
 X 2 LINES  
 (20 DWA/LINE)

 MEM MAP  
 160 X 2 BITS/LINE  
 X 2 LINES  
 (40 DWA/LINE)

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GAME OR PROJECT

ANTIC

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MODE

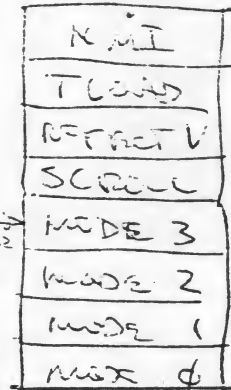
mode



- ~~NMI~~
- ~~REFLECT H~~
- REFLECT V
- SCROLL
- TLOAD
- MODE 2
- MODE 1
- MODE 0



EXTEND COLOR



### MODE SUMMARY TO DATE

CLOCK = 3.58 MHz

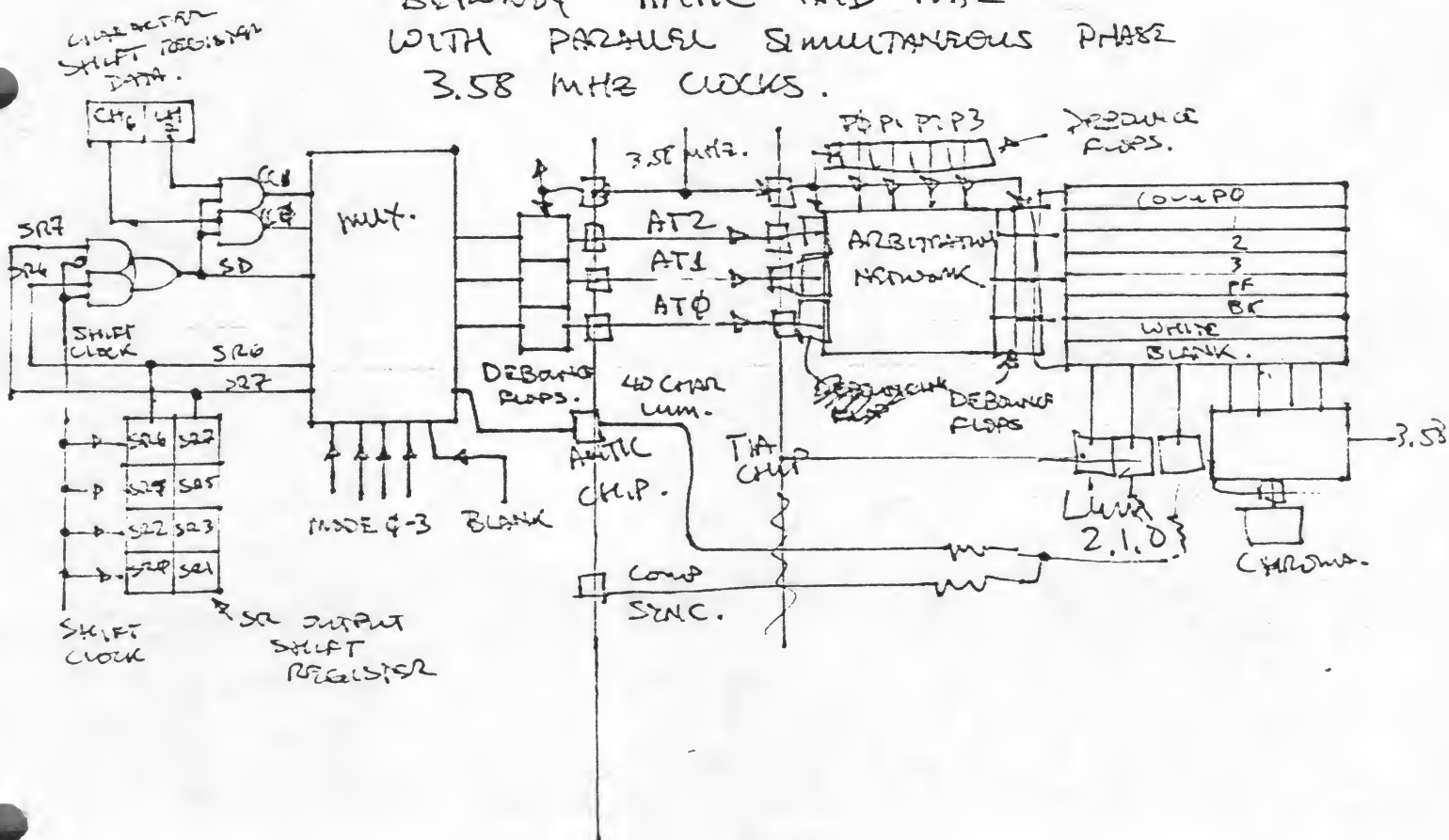
CODE ?	MODE	DESCRIPTION	ELEMENT SIZE
	BLANK	16NES LINES BLANK	<del>16NES</del> LINES.
	20 CHAR 1	8x8+1 CHAR + 2 COLOR BITS	8 LINES x 8 CLOCKS
	20 CHAR 2	" "	8 PAIRS x 8 CLOCKS
	20 CHAR 3	8x8+2 CHARACTER	8 LINES x 8 CLOCKS
	20 CHAR 4	" "	8 PAIRS x 8 CLOCKS
	40 CHAR	8x8+1 CHAR + 1 INVERT BIT.	10 LINES x 8 1/2 CLOCKS.
	40 CELL 1	40 (1 BIT SQUARES)	8 LINES x 4 CLOCKS
	40 CELL 2	40 (2 BIT SQUARES)	
	80 CELL 1	80 1 BIT SQUARES	4 LINES x 2 CLOCKS
	80 CELL 2	2 BIT SQUARES	
	160 CELL 1	1 BIT SQUARES	2 LINES x 1 CLOCK.
	160 CELL 2	2 BIT SQUARES	

GAME OR PROJECT  
**ANTIC** VIDEO COMMUNICATION TO TIA2

6 COLOR LUM REGISTERS IN TIA2.

AT2	AT1	AT0		
1	0	0	COLUMN P0	P0, 20 CHAR x 4 COLS
1	0	1	COLUMN P1	P1, 20 CHAR x 4 COLS
1	1	0	COLUMN P2	P2, 20 CHAR x 4 COLS, EXTENDED COLS
1	1	1	COLUMN P3	P3, 20 CHAR x 4 COLS, EXTENDED COLS
0	0	1	COLUMN PF	MAX 40 COLS, 2 COLS, EXTENDED COLS
0	0	0	COLUMN BK	DEFAULT - " " " , BLANK MODE
0	1	0	FORCE WHITE	40 CHAR MODE
0	1	1	FORCE BLANK.	HOR U BLINKING

3 COMMUNICATION LINES BETWEEN ANTIC AND TIA2 - WITH PARALLEL SIMULTANEOUS PHASE 3.58 MHz CLOCKS.



GAME OR PROJECT

JOHN ET

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EXAMPLE A 300000  
 BASIC SUPER MACHINE  
 53 KEYS.

100 FOR  
 WITH POWER  
 100 FOR  
 WORKING  
 WITH POWER

40 ~~KEYS~~ KEYS OF RAM. 4K ROM.  
 4K RAM EXPANSION FOR MS.  
 MULTIPLEXED SYMMETRIC PANS INTERIOR.

3 JACKS ON BACK FOR TAPES AND AC.  
 (IDENTICAL IN APPEARANCE!)

ONE EXPANSION BUS CONNECTOR. (40 PIN)

300 BAUD TAPE FORMAT.

GRAPHICS ARE BLACK & WHITE  
 CHARACTERS, 1 LEVEL, 16x16

OR 128x48V. GRAPHICS.

HIS MONITOR THAT YOU CONTROL  
 BY SINGLE KEY.  
 TAPE LOADED PROGRAMS AND  
 WRITTEN IN BASIC. ~~ALSO~~  
 ALLOWS YOU TO LIST THE PROGRAM.

EXTERNAL TRANSFORMERS. (BEHIND) REFRIGERATORS,  
 CAPACITORS. (NO AC APPROVAL)

POW. SUP. 50W. 12A 17AC  
 100V 1000V



82

GAME OR PROJECT

6579

George Rice?

SYNTHETIK

ADVICE

BILL BRUGES

GEORGE RICE

BOB BRUNER

JERRY DENNEY

MICHAEL ASBIE

LOOK AS SYNTHETIK'S LIST FIRST.

SINGLE FACT LINE -  
PARTS PROCESSOR AND  
TRI STATES BUSSES.

ASK FOR A SPECIFICATION  
BETWEEN  $\phi_0$  IN,  $\phi_1$  OUT,  $\phi_2$  OUT.

P. C, V, I, Z, N, D, B.

MOVE BREAK TO SEPARATE  
VECTOR - UNLOAD 2201K BIT.

ADD HALF CARRY

~~ADD~~  
ENABLE AUTO INCREMENT.

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GAME OR PROJECT  
2559

JMP 052 IMMEDIATE

JMP 050 (IMMEDIATE)

JMP 052

---

JMP RELATIVE  
052 RELATIVE

---

TPA TP

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GAME OR PROJECT

GREEN

JAMES REPORT FROM  
PADARO

4K RAM

ROM CASSETTE UNIT BK or 400002

CSDZ (MAYBE CSDZ)

PULSE &amp; RESIDENT KEYBOARD

VIA &amp; SERIAL EXPANSION

84K RESIDENT ROM?

NO RESIDENT CASSETTE

(RAM CASSETTE)

ANAL &amp; 4-BIT TIA

2 CASSETTE JACKS -

W/MOTOR START STOP

AUTOMATIC REWIND?

LIGHT PEN

AUDIO AND DIGITAL ON TAPES

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JOY SAYS 6509 IS

BIG MAFK, BECAUSE OF TIME.

WHAT IS SENSITIVITY OF SCHEDULE  
VS FEATURES.

HOW FAST CAN WE BRING  
UP OTHER VENDORS.

HOW ABOUT OTHER <sup>PROCES</sup> ~~THESE~~ VENDORS  
LIKE MIC AND FANT?

GAME OR PROJECT

ATARI 2600 - COLOR TV SET

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ADDRESS RANGE

DATA

	C2	C1	C0	DATA
1	0	0	1	000000
1	0	1	1	000001
1	1	0	1	000010
1	1	1	1	000011
0	0	0	1	000100
0	0	0	0	000101
0	1	0	0	000110
0	1	1	1	000111

PO - OR TO CHAR BY COLOR

PI

PC

PD

PE

PF

ENTERED  
COLOR CHAR  
OR NAME

DEFAULT - TOP LEVEL CONTROL UNIT

ALL TRANSMISSION ON

ALL TRANSMISSION OFF (TO CHAR SW)

\* GR7 @  
CH9

INITIAL MODES

CODE	MODE	C2	C1	C0
	BLANK	0	0	0
1 0 1	20CH 20H1	SG	CH7.SG	CH6.SG
1 0 1	20CH 20H2	GR7	GR7*	GR4
1 1 0	20CH 20H3	SG	CH7.SG	CH6.SG
1 1 1	20CH 20H4	GR7	GR7*	GR6
<del>1 1 0</del>	<del>40CH</del>	<del>0</del>	<del>1</del>	<del>1</del>
<del>1 1 1</del>	<del>40CH 20H1</del>	<del>0</del>	<del>0</del>	<del>SG</del>
1 0 0 1	40CH 20H5	GR7	GR7	GR6
1 0 1 0	80CH 20H1	0	0	SG
1 0 1 1	80CH 20H2	GR7	GR7	GR6
1 1 0 0	160CH 20H1	0	0	SG
1 1 0 1	160CH 20H2	GR7	GR7	GR6
1 1 1 0	160CH 20H3	0	0	SG
1 1 1 1	160CH 20H4	GR7	GR7	GR6

BLANK NL

20CH502L

20CH401L

20CH402L

40CH

40D208L

40D408L

80D204L

80D404L

160D202L

160D402L

160D201L

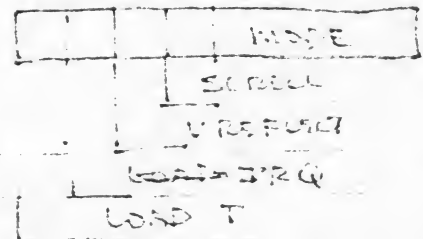
160D401L

MODE = 000 = EXTENDED COLOR

MODE

MODE - CHARACTER SET

DISPLAY LIST  
CONTROL OF CODE





GAME OR PROJECT: ANTIC      ADDRESS GENERATOR.

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- BC [7 6 5 4 3 2 1 0]      BIT 7 POINTER FOR CHARACTERS
- SR [7 6 5 4 3 2 1 0]      OUTPUT OF CHARACTER BUFFER.
- X [8 7 6 5 4 3 2 1 0]      DISPLAY LIST POINTER.
- T [15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0]      MEMORY LATCH.      BINARY DIVIDER COUNTER.      SCANNER - COUNTER.
- A [2 1 1 0]      BLANK 3 BIT LINE-DOWN COUNTER.
- H [8 7 6 5 4 3 2 1 0]      HORIZONTAL SYNC COUNTER.
- V [8 7 6 5 4 3 2 1 0]      VERTICAL SYNC COUNTER.

R/C RIGHT-LEFT BIT SELECT FOR 256 OR 20 CHANNEL X 4 COLOR MODE. - DERIVED FROM HZ

TYPE OF CYCLE	MODE	ADDRESS BUS
BLANK N	0 0 0 0	
40 CH	0 0 1 0	BC7 6 5 4 3 BC2 SR6 5 4 3 2 1 0 A2 1 0
20 CH 5COL 1L	0 1 0 0	BC7 6 5 4 3 2 BC1 SR5 4 3 2 1 0 A2 1 0
20 CH 4COL 1L	0 1 0 1	BC7 6 5 4 BC3 SR7 6 5 4 3 2 1 R/C " " "
20 CH 5COL 2L	0 1 1 0	BC7 6 5 4 3 2 BC1 SR5 4 3 2 1 SRP " " "
20 CH 4COL 2L	0 1 1 1	BC7 6 5 4 3 SR7 6 5 4 3 2 1 R/C A2 1 0
40 CELL 2COL 8L	1 0 0 0	T LATCH      T COUNTER T11 - T0
40 CELL 4COL 8L	1 0 0 1	15 14 13 12      "
80 CELL 2COL 4L	1 0 1 0	"      "
80 CELL 4COL 4L	1 0 1 1	"      "
160 CELL 2COL 2L	1 1 0 0	"      "
160 CELL 4COL 2L	1 1 0 1	"      "
160 CELL 2COL 1L	1 1 1 0	"      "
160 CELL 4COL 1L	1 1 1 1	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 7 0
REFRESH		0 0 0 0 0 0 0 0 0 14 13 12 11 10 9 8 7 6
MODE FECH.		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0
OBJECTS		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 0

GAME OR PROJECT  
 ANTIC TIA OBJECT COLLISIONS:

TIA OBJECTS

TIA VIDEO:

- TP0 -
- TP1 < DECODES GENERATED.
- TP2
- TP3
- TBD } DECODES GENERATED

ANTIC VIDEO

ECODES	APF	CODE # 1	2 COLOR SCREEN AND 4 COLOR SCREEN
FROM	AP0	CODE 4	5 COLOR CHAR OR 4 COLOR CHAR
ANTIC	AP1	CODE 5	"
VIDEO	AP2	CODE 6	5 COLOR CHAR, 4 COLOR CHAR, OR 4 COLOR S
EXCLUSIVE	AP3	CODE 7	"

ANTIC VIDEO MODES ARE EXCLUSIVE -  
 SO NO COLLISIONS NEED BE DETECTED AMONG THEM.  
 THE BOARD GENERATOR CAN BE CLASSED WITH THE  
 PLAYFIELD. - SINCE NO COLLISIONS ARE OF SIGNIFICANCE  
 EXPECTED BETWEEN IT AND ANTIC  
 GENERATED OBJECTS.

	APF	AP0	AP1	AP2	AP3	TBD	APF	AP1	AP2	AP3
AP3	0	0	0	0	0	X	X	X	-	-
AP2	0	0	0	0	0	X	X	-	-	-
AP1	0	0	0	0	0	X	-	-	-	-
AP0	0	0	0	0	0	-	-	-	-	-
TBD + APF	0	0	0	0	0	-	-	-	-	-
TP3	0	0	0	0	0	-	-	-	-	-
TP2	0	0	0	0	0	-	-	-	-	-
TP1	0	0	0	0	0	-	-	-	-	-
TP0	-	-	-	-	-	-	-	-	-	-

20 COLLISIONS BETWEEN 4 TIA  
 OBJECTS AND 5 DIFFERENT  
 EXCLUSIVE DECODES.

6 MUTUAL COLLISIONS AMONG  
 4 TIA MOVING OBJECTS.

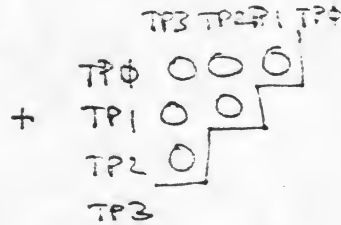
GAME OR PROJECT

ANTIC - TIA COLLISIONS - CONT.

CONFIDENTIAL

26 COLLISIONS.

	APF	AP2	AP1	AP2	AP3
TP0					
TP1					
TP2					
TP3					



?

CTP0T	AP3	AP2	AP1	AP0
CTP1T	AP3	AP2	AP1	AP0
CTP2T	AP3	AP2	AP1	AP0
CTP3T	AP3	AP2	AP1	AP0

16 COLLISION LATCHES APPEAR TWICE

INTERFERED WITH 4 APF COLLISIONS.

CTP0A	AP3	AP2	AP1	AP0
CTP1A	AP3	AP2	AP1	AP0
CTP2A	AP3	AP2	AP1	AP0
CTP3A	AP3	AP2	AP1	AP0

LOOKS LIKE 32 BITS.

OR 4 BYTES, OR 16 PAIRS

16 PAIR CONFIGURATIONS.

BIT 7 BIT 6

TP0	APF	AP0
TP0	TP1	AP1
	TP2	AP2
	TP3	AP3
TP1	TP0	AP0
TP1	APF	TP1
	TP2	AP2
	TP3	AP3
TP2	TP0	AP0
TP2	TP1	AP1
	APF	AP2
	TP3	AP3
TP3	TP0	AP0
TP3	TP1	AP1
	TP2	AP2
	APF	AP3

OR

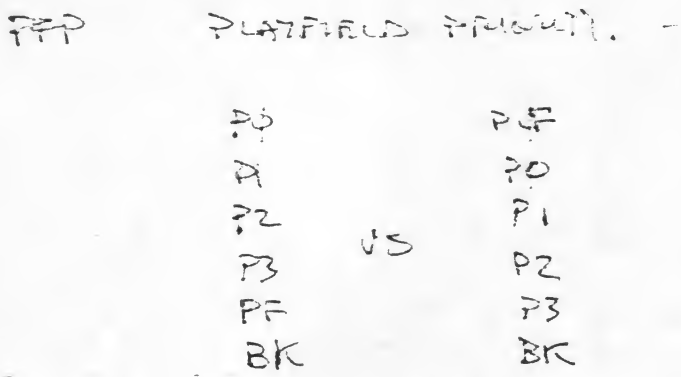
TP0	APF	TP0
TP1	TP0	TP1
TP2	TP0	TP2
TP3	TP0	TP3
TP0	TP1	TP0
TP1	APF	TP1
TP2	TP1	TP2
TP3	TP1	TP3
TP0	TP2	TP0
TP1	TP2	TP1
TP2	APF	TP2
TP3	TP2	TP3
TP0	TP3	TP0
TP1	TP3	TP1
TP2	TP3	TP2
TP3	APF	TP3

GAME OR PROJECT

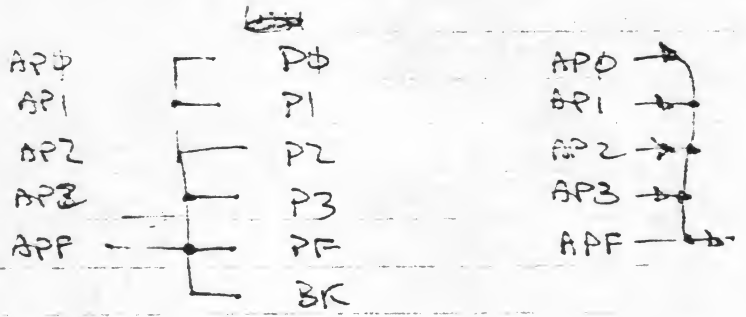
ANTIC-TILE, PRINTOUT, 2-24-77

CONFIDENTIAL

CONTROL BITS.



ATC ANTIC COLOR.



GAME OR PROJECT  
T.A.Z PINS AND ADDRESSES

CONFIDENTIAL

a T.A.Z CONTAINS

4 8 BIT LATCHES

~~6~~ 6 COLOR/BACKGROUND REGISTERS.  
COLLISION LATCHES

WRITE  
ADDRESSES

COLUP $\phi$ , 1, 2, 3	4
GRP $\phi$ , 1, 2, 3	4
HPOS $\phi$ , 1, 2, 3	4
MUSIZ $\phi$ , 1, 2, 3	4
VDLCP $\phi$ , 1, 2, 3	4
	<u>20</u>

+ 16 COLLISION

READ ADDRESSES

COLUPF	
<u>COLUBK</u>	
CTRLPF	
<u>CTRLBD</u>	
CTCLR	5
	<u>25</u>

<32

PINS	VSS, VCC	2
	CLK (3.5K)	1
	SYNC (ANTIC)	1
	RIW, $\phi$ 2	2
	D $\phi$ -D7	8
	A $\phi$ -A4	5
	$\overline{CS}$	1
	A $\phi$ , 1, 2	3
	LUM $\phi$ , 1, 2	3
	CHROMA, DEL	2
		<u>28</u> !!!

WRITER	JOSEPH DEWILL	DATE	3/8/82	WITNESS		DATE	
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GAME OR PROJECT

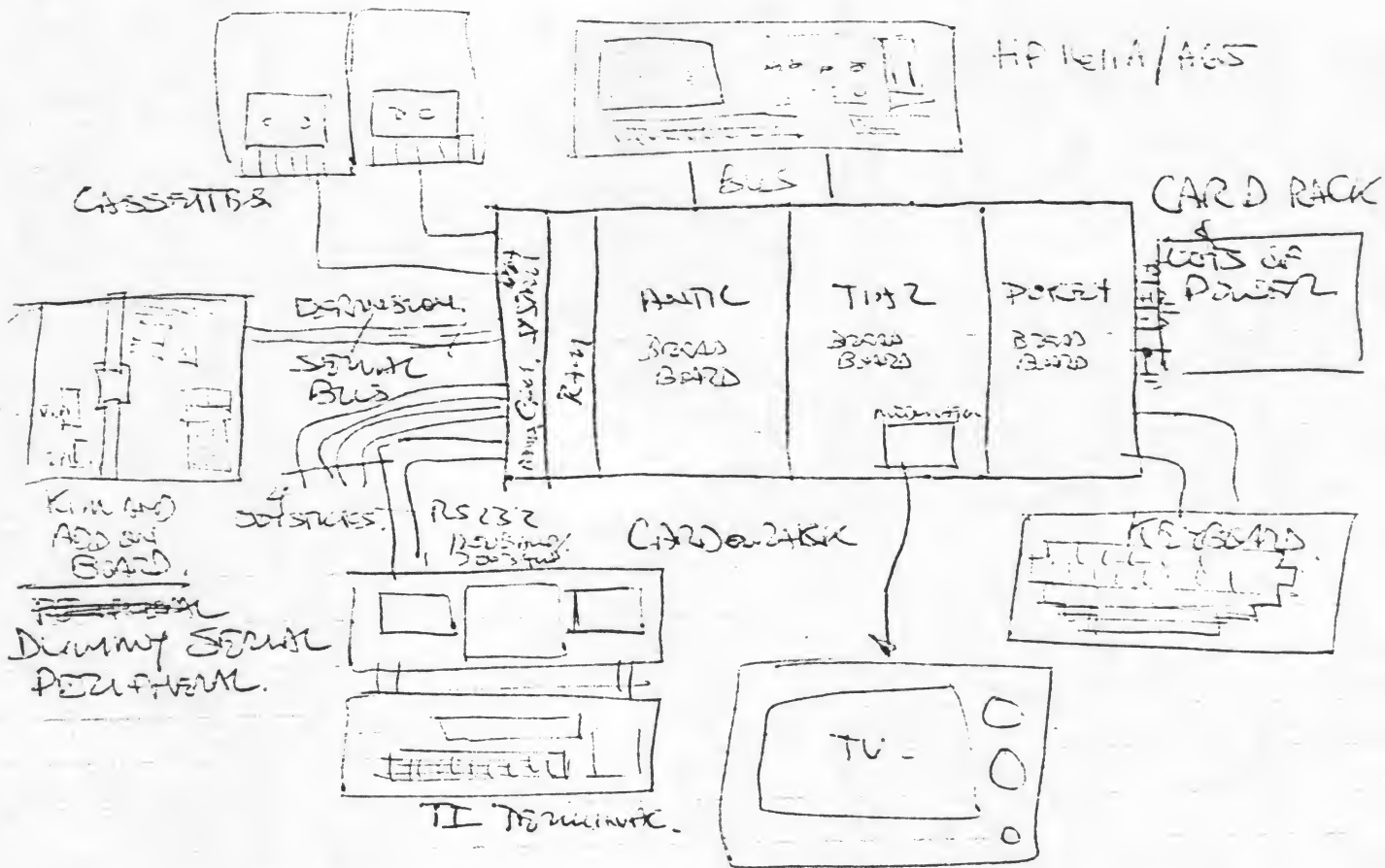
DEVELOPMENT SYSTEMS FOR COLLEEN

CONFIDENTIAL

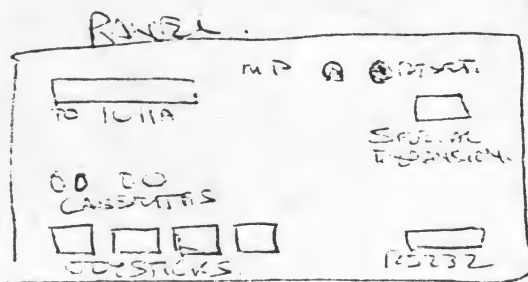
CONCEPT:

FOR CHIP DEVELOPMENT,  
AND EARLY SOFTWARE DEVELOPMENT:

2 COMPLETE METHODS.



1011A FOR LOGIC ANALYSER, DEBUG.  
TI FOR LOAD/STORE TAPES.



SYSTEM BOARD INCLUDES.

- CPU.
- BUS BUFFERS.
- VIA FOR JOYSTICKS, TAPE I/O, SERIAL PORT
- TAPE I/O
- 1011A FOR TI INTERFACE
- PROMS WITH DEVELOPMENT MATERIAL (IE: 64K BUS AND SO)

WRITER

Joe DeLuca

DATE

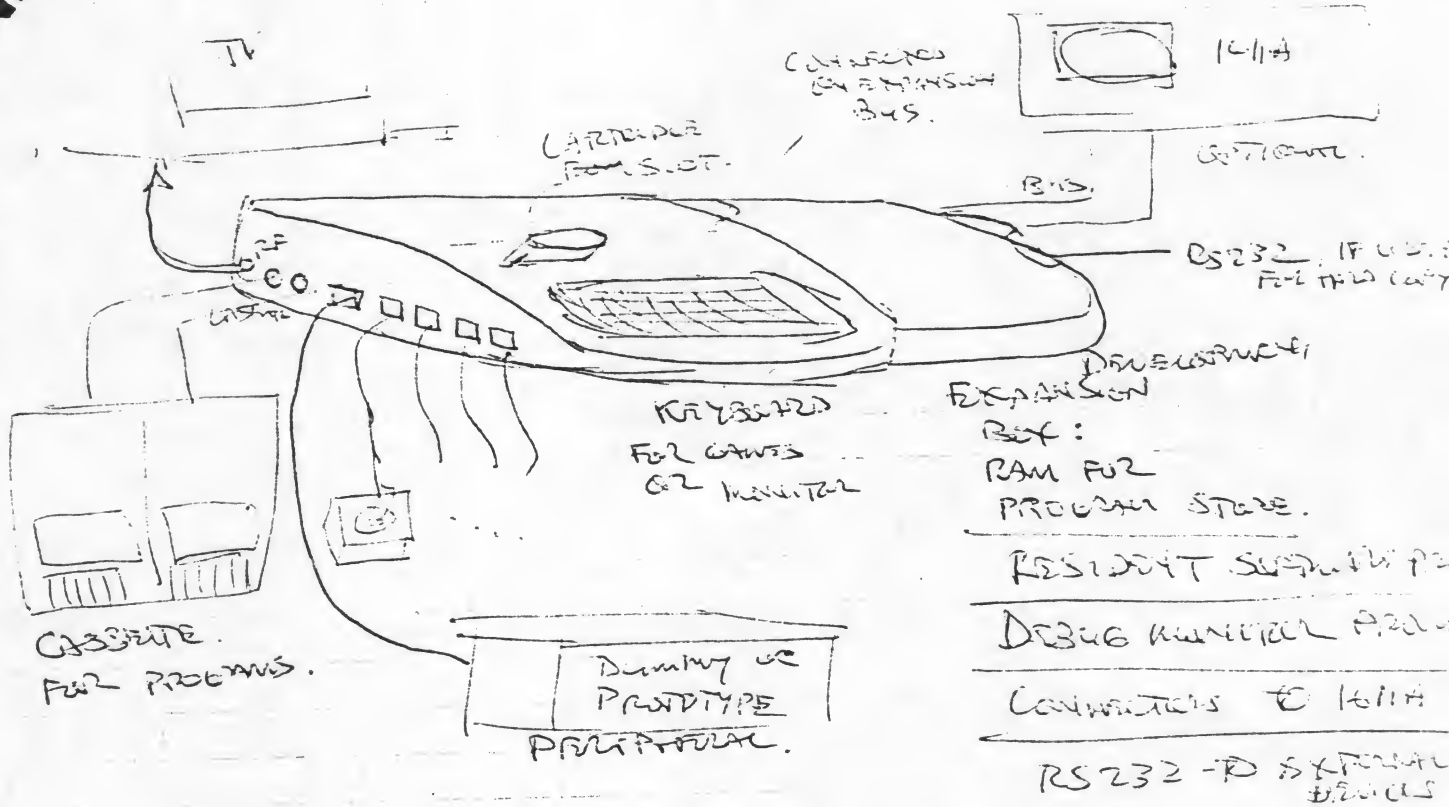
6-1-81

WITNESS

DATE

CONFIDENTIAL

CONCEPT FOR PRODUCTION SOFTWARE DEVELOPMENT UNITS.



BUILD A WORKING COLLECTOR UNIT.

CONNECT TO THE EXPANSION BUS.  
 ADD A BOX THAT ALLOWS LOADING AND DEBUGGING OF APPLICATIONS PROGRAMS. - USE RESIDENT KEYBOARD AND TV SCREEN FOR COMMUNICATION w/ DEBUG MONITOR.

GAME OR PROJECT

ANTIC POKEY

CONFIDENTIAL

PINOUTS. ANTIC

2	VCC, VSS	POWER	POWER AND CLOCKS.
1	CLK	3.58 CLOCK	
2	Φ1 Φ2	CLOCKS TO MEMORY	
2	TSC, RW	BUS CONTROL	POKEY SIGNALS
1	INT	INTERRUPT OUT (TO MEMORY)	BUS
1	CS	REGISTER CHIP SELECT.	SIGNALS
8	DB0-DB7	DATA BUS.	
16	AB0-AB15	ADDRESS BUS	
1	SYNC	SYNC SIGNAL TO TIA2	VIDEO.
3	AUΦ1,2	VIDEO TO TIA2	
2	CSTN, L40	COMPOSITE SYNC, 40 CH. LUM OUT.	
39	PINS		
1	LP.	LIGHT PEN ?	
40	<del>TO POKEY</del>		IN POKEY.

PINOUTS. POKEY.

2	VSS, VCC	POWER	POWER AND CLOCKS
1	Φ2	CLOCK	
1 ?	SYNC	HORIZONTAL FROM ANTIC	
1	INT (00)	POKEY INTERRUPT REQUEST.	
2	CS	CHIP SELECT	INPUT
4	AB0-AB3	ADDRESS INPUTS	BUS.
8	DB0-DB7	DATA BUS	SIGNALS.
1	RW		
8	PA0-PA7	POT INPUTS.	40
8	KA0-KA7	KEY BOARD INPUTS	
12 } 3	KB0,1,2	ENCODER (JOYSTICK) SCAN OUTPUTS.	
1	AND	AND	
39	PINS		
40	<del>TO ANTIC</del>		



94

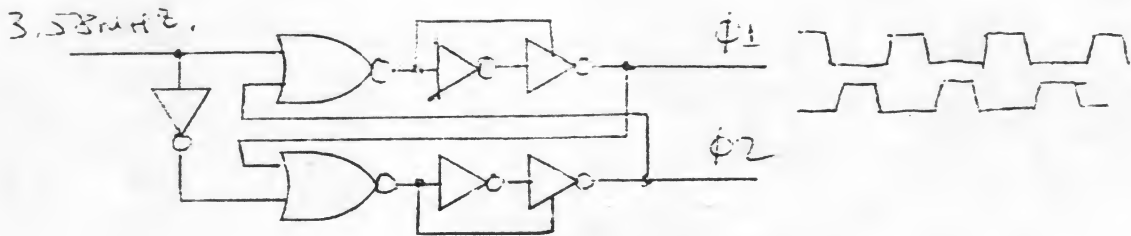
GAME OR PROJECT

ANTIC

CONFIDENTIAL

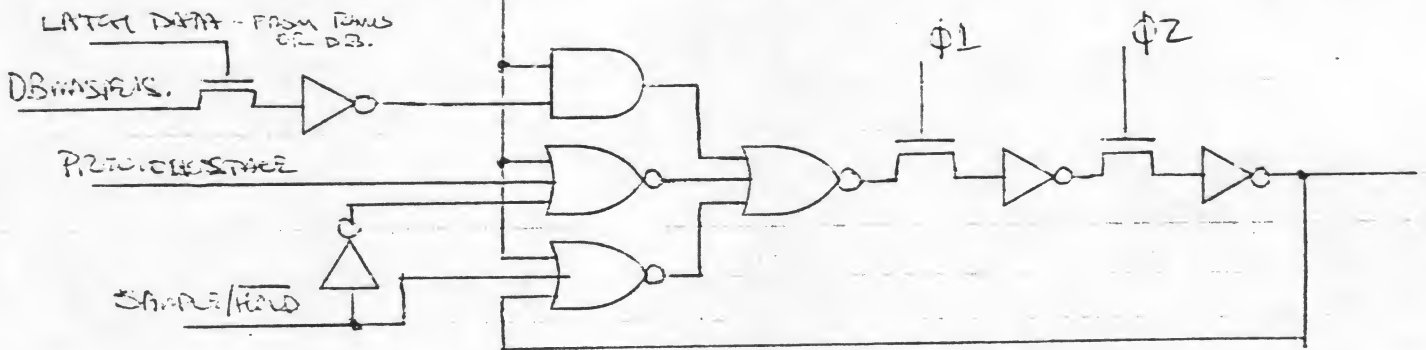
2 CELLS

$\Phi$   $\Phi_1$   $\Phi_2$  SPUNTER R2 355 USED IN ADDRESS



OUTPUT SHIFT REGISTER CELL.

LOAD - DELAYS  $\Phi$ -7 SHIFT CLOCKS.





GAME OR PROJECT

ANTIC COURSE

CONFIDENTIAL

CONVERSATION WITH

ANTIC PINS

DONT PUT COUNT FOR ANTIC

DONT GET THE SEPARATE SYNC TO TIA -  
US GET PIN -

AND BUFFER COUNTERS WITH - USE  
LEFT TRIG.

-> ANTIC HAS 30 PINS

-> 2 PINS FOR DMA COUNT, DMA REQUEST.

STEVIE SUGGESTS SCROLLING

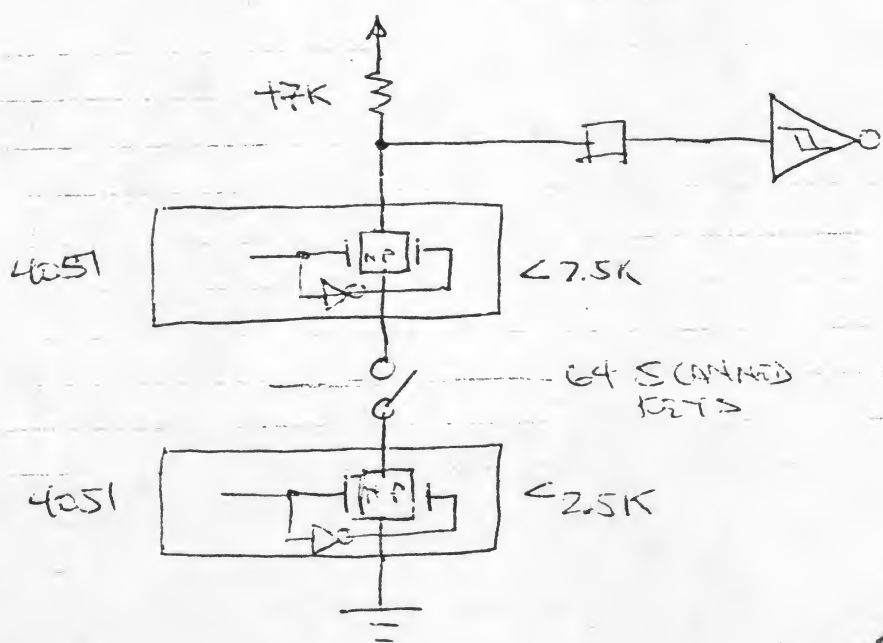
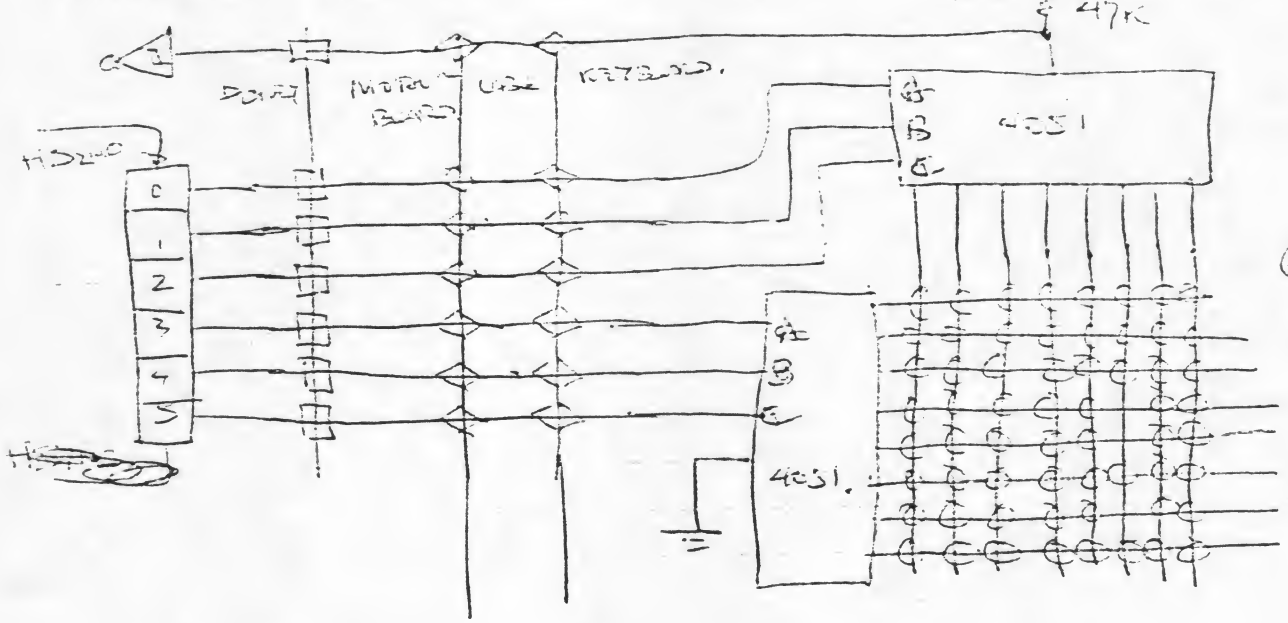
WHOLE SCREEN BY SHIFTING

SYNC AND BLANK

LEAVE OUT OTHER SCROLLING

GAME OR PROJECT  
 KEY - KEYBOARD

WASTE DO KEYBOARD WITH TWO MIXERS - 4051B CIRC



$$\frac{5}{5+47} = \frac{5}{52} \times 5.01 \approx$$

**CONFIDENTIAL**

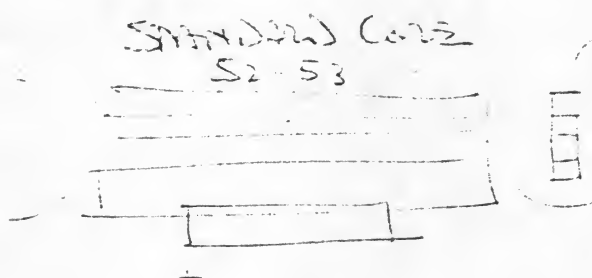


GAME OR PROJECT ~~Keyboard~~ KEYBOARD MACHINE

CONFIDENTIAL

KEY DIAGRAM

W/ 200K APP  
REWIN MONITOR  
DATA INPUT



4/SIDE  
5/SIDE  
3/SIDE

STANDARD CASE  
52-53

5 CURSOR  
4 MAT GAMES  
SS GAMES  
TRACE GAMES  
60 OPTIONS

75-304 / KEY

RESET  
10 COMPUTER CONTROL

CAN THIS USE STD  
STRUCT CONTROLS

$$\frac{5 + 52-53 + 5}{63}$$

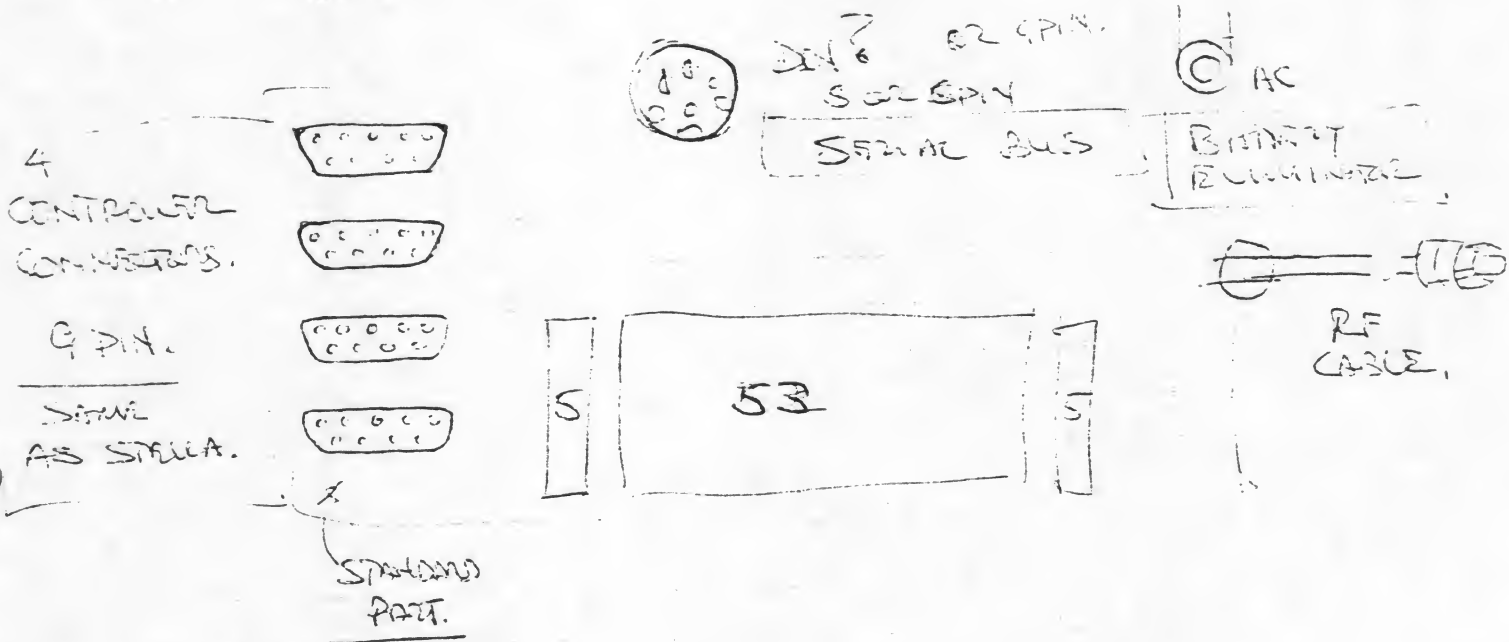
$$53 + 10 \pm 6$$

"KEYBOARD MUST BE SET" ems

FANCY GAME PAYOR THAT  
YOU CAN PLAY IT IN BASIC

GAME OR PROJECT  
CONFIDENTIAL

JOHN ELLIS ACCEPTS IDEA  
OF PUTTING SIGNALS  
FOR CASSETTE INTO CASSETTE



**CONFIDENTIAL**

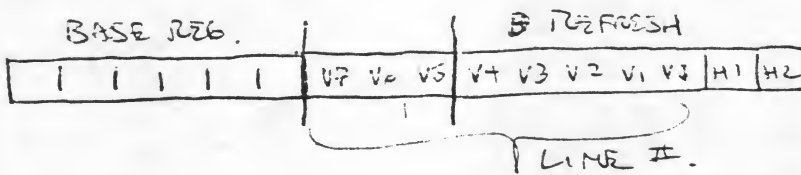
GAME OR PROJECT  
ANTIC, TIA.

FOR AUTOMATIC OBJECT GENERATION:

TAKE REFRESH CYCLES.

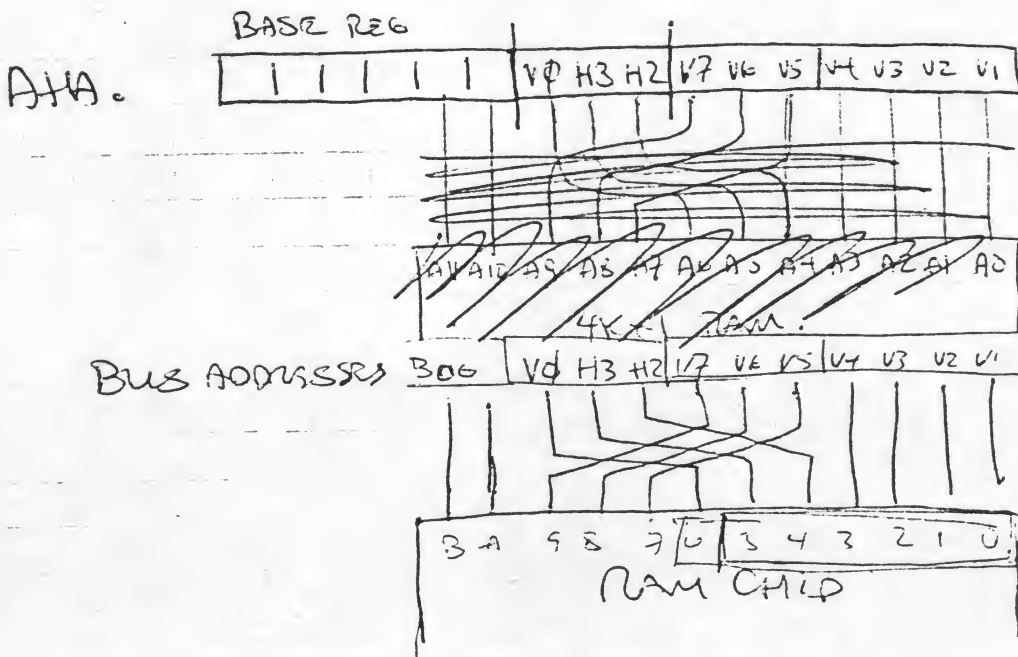
HAVE TIA RECOGNIZE THEM

ADD BASE POINTER TO REFRESH.



FOR FETCHING OBJECT GRAPHICS OUT OF MEMORY.

TIA CAN ACCEPT THESE GRAPHICS

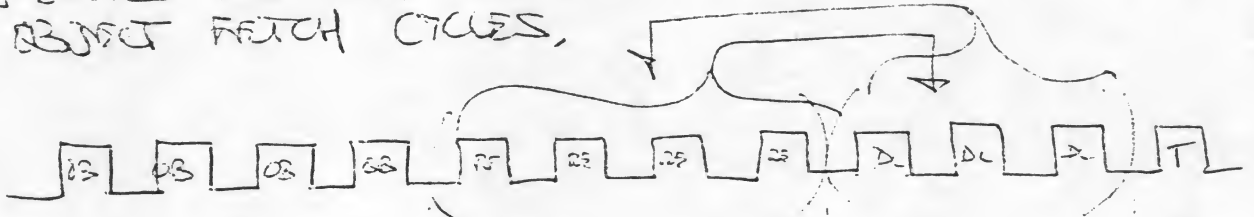


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GAME OR PROJECT  
**ANTIC / TIA2**

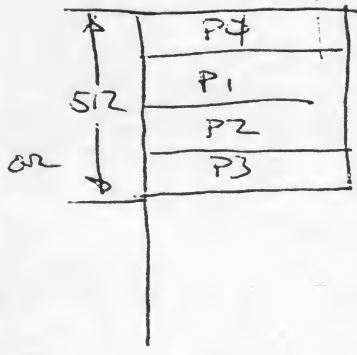
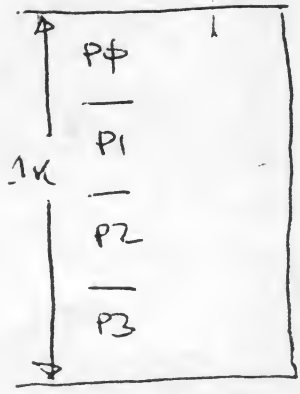
**OBJECT GENERATION**

SEPERATE REFRESH CYCLES FROM  
 OBJECT FETCH CYCLES,



AB 15	OBL15	X	0	TL15
14	OBL14	X	0	TL14
13	OBL13	X	0	TL13
12	OBL12	X	0	TL12
11	OBL11	X	0	TL11
10	OBL10	X	1	TL10
9	H3 or OBL9	X	DLC 9	TL9
8	H2 or H3	X	DLC 8	TL8
7	OBC7 or H2	V5	DLC 7	TL7
6	OBC6	V4	DLC 6	TL6
5	OBC5	V3	DLC 5	TL5
4	OBC4	V2	DLC 4	TL4
3	OBC3	V1	DLC 3	TL3
2	OBC2	V0	DLC 2	TL2
1	OBC1	H3	DLC 1	TL1
0	OBC0	H2	DLC 0	TL0

TABLES  
 OF  
 OBJECTS



GAME OR PROJECT  
TIA2 / ANTIC.

VERTICAL SYNC DELAY. IN 128 BYTE TABLE

CONFIDENTIAL

OBJECT DATA DATA.

LINE	Z <sub>N</sub>	P <sub>1</sub> N	P <sub>2</sub> N	P <sub>3</sub> N	
	Z <sub>N+1</sub>	P <sub>1</sub> N	P <sub>2</sub> N	P <sub>3</sub> N	P <sub>1</sub> , P <sub>2</sub> NOT DELAYED
	Z <sub>N+2</sub>	P <sub>1</sub> N+1	P <sub>2</sub> N+1	P <sub>3</sub> N+1	P <sub>1</sub> , P <sub>2</sub> DELAYED
	Z <sub>N+3</sub>	P <sub>1</sub> N+1	P <sub>2</sub> N+1	P <sub>3</sub> N+1	
	Z <sub>N+4</sub>	P <sub>1</sub> N+2	P <sub>2</sub> N+2	P <sub>3</sub> N+2	
	Z <sub>N+5</sub>	P <sub>1</sub> N+2	P <sub>2</sub> N+2	P <sub>3</sub> N+2	

IF NOT DELAYED, CAPTURE OF 1ST LINE.  
IF DELAYED, CAPTURE OF 2ND LINE.

REGISTERS IN ANTIC. FROM CPU POINT OF VIEW.

WRITE	BC	X
WRITE	OB <sub>3</sub>	X
WRITE	TC counter low.	
WRITE	TLATCH / TC HIGH	
R/W	TVAR2 (?)	
READ	V counter	
READ	STATUS.	
WRITE	START. TIA2 CONTROL.	
WRITE	<del>XXXXXXXXXX</del>	
WRITE		
WRITE	DLCH	
WRITE	DLCH	

BASE ADDRESS CHANNELS,  
BASE ADDRESS OBJECTS,  
MEMORY POINTER "T"

} READ VERTICAL COUNTER  
INTERRUPT BITS. ETC.

HORIZONTAL OFFSET  
MODE (DMA)



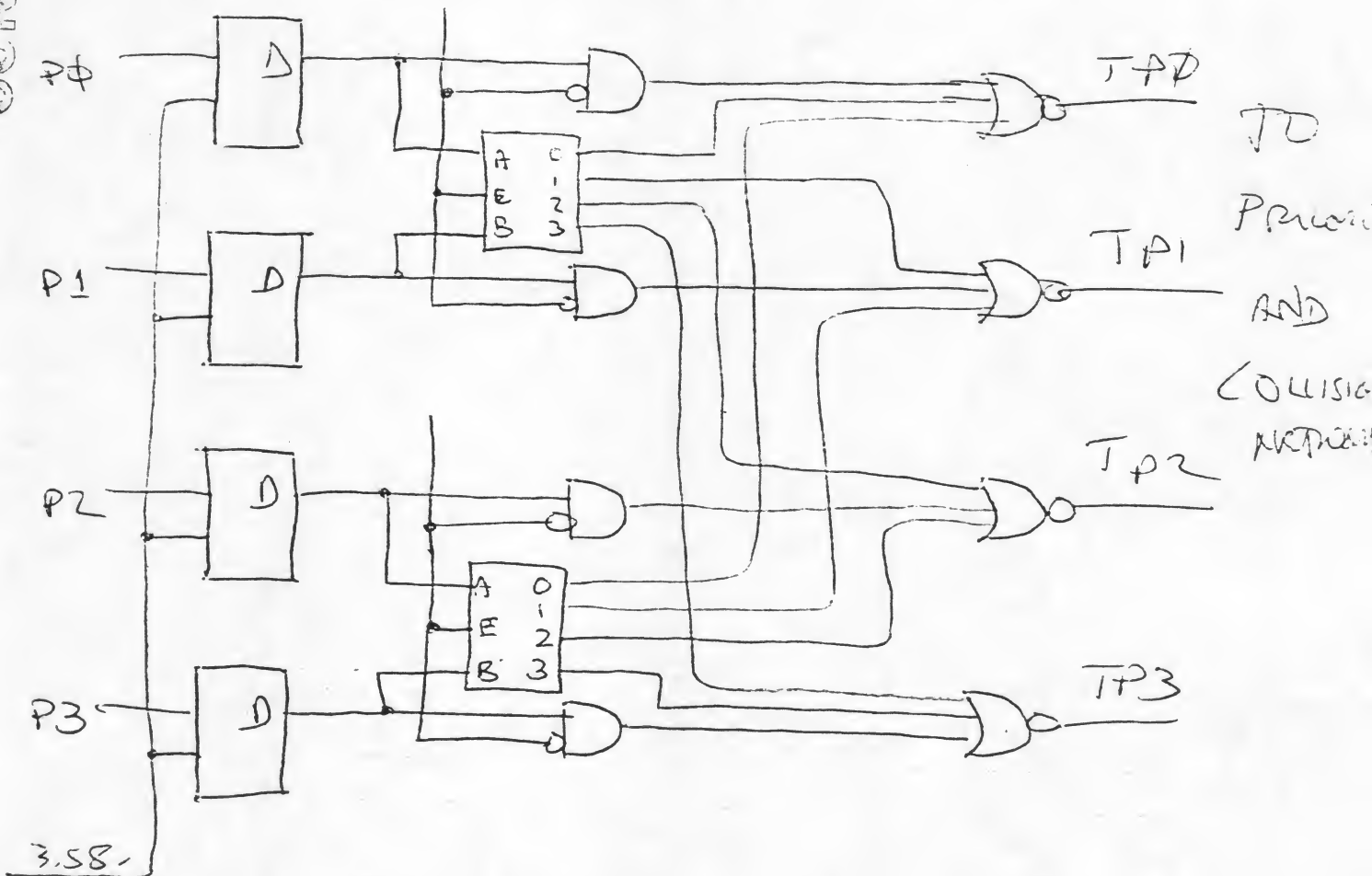
GAME OR PROJECT

TIA

CONFIDENTIAL

ANOTHER HOT IDEAS.

CHANGE TWO 8 BIT TIA OBJECTS TO BEHAVE INTO ONE 4 COLOR/POINT OBJECT



EACH OBJECT CAN BE INDEPENDANT (ONE LEVEL) OR PAIRED (TWO LEVEL)

WRITER

DELUIR

DATE

23 NOV 77

WITNESS

Jay Thomas

DATE

GAME OR PROJECT

CALIFORNIA PARADISE MEETING

29 NOV 77

JOE WANTS TO  
DEFINE THE PRODUCT,  
AND GET IT OUT.

TWO CARTRIDGES.

STILL - QUOTES FROM ME.

KEYBOARD	04 \$16	(-53 + 5 + 2)	6502	5.0
	32 \$8		RAM 4K	12.8
			RAM 4K	3.00
			U.A	3.0
TOTAL PARTS	\$115.17		ANTIC	6.00
LABOR	12		TIA	7.50
LOSS TO BUILD	127.17	=> 300!!	POWER	4.00
			MSI	7.50
				<u>40.80</u>

"STUCK WITH THIS."

PROPOSED SOLUTIONS.

TWO PROPOSED PRODUCTS

GAME PLAYER, NON EXPANDABLE = TOTAL PARTS

"CANDY" PARTS \$85.50 NO KEYBOARD  
 + 9 = \$94.50 NO INTERFACE  
 ONE CONTROLLER CAPABILITY. SAME IC

BUILT STILL  
NOT FCC  
APPROVED

DESIGN BUT MAY NOT INTRO DICE  
 CALIFORNIA + BUILT IN COLOR MONITOR

"ELIZABETH" \$100 13" COLOR MONITOR  
 PARTS \$211 + 12 = \$500

CONFIDENTIAL

GAME OR PROJECT

COWBOY / CANDY / ELIZABETH

TRY BEST TO BUILD SPELDS  
INTO 1979!

ALSO  
AT WORK  
EUIS  
THING

JOE SEES THE SET

FCC PROBLEM w/ COWBOY  
UL PROBLEM w/ ELIZABETH.

IF CHIP SET AVAILABLE IN NOV 78  
WE CAN SHOW IN JANUARY.

JOHN BURICH SUGGESTS  
THAT JAPANESE MAY PUT  
VIDEO INPUT ON FUTURE TV'S,

LOTS OF CHATTER.

PENHAPS

ADD SERIAL PORT TO CANDY  
DELETE COWBOY  
BUILD ELIZABETH.

CONFIDENTIAL

GAME OR PROJECT

COURT @ ADARO.

CONFIDENTIAL

72K BYTES MEMORY

RESISTANCE

JACK BOURTO  
GERTZ REED  
MUR ASSAR.

MINUTES, PERIPHERALS & MICROS.

DID NOT GET INTO DYNAMIC RANGE

(USING POLYSILOXANE RESISTORS  
IN PLACE OF DEPLETION LOADS)  
WASTED \$\$\$ IT, TOO

WORKING ON H-UOS.

16K STATIC !! 4Kx4, or 2Kx8  
200 NSEC IS "SLOW"

JACK SAYS \$300 2114 in 1979

70MG, 350 SEC.

WORKING FOR 4Kx15.

66509 - COMPUTATION 142 52MG.

GAME OR PROJECT

PALMTO - SYNTEK MEETING CONTINUED

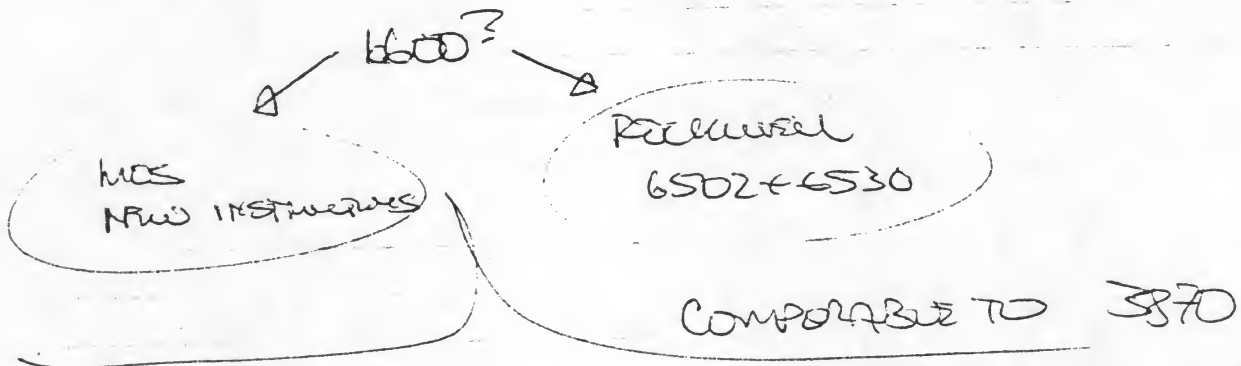
6551 - ACIA

6509

CRT CONTROLLER

FLOPPY DISK CONTROLLER

DID NOT AGREE ON 6600!!!



OUR DISCUSSIONS:

DESIGN FOR M6512  
 PUSH DEVELOPMENT OF S6519/09  
 MAKE DECISION LATER TO USE 6519 OR 12.

CONFIDENTIAL

GAME OR PROJECT

PADAW, SYNERGIC

CONFIDENTIAL

6502

M6502

S6509

SOFTWARE COMPATIBLE

UPWARD SOURCE COMPATIBLE.

BC  
TALT.

TSC  
TALT.

INWARD COMPATIBLE.

NOT NECESSARY TO BE FINANT.

1ST PARTS ON M6502 END  
1ST QUARTER.

QUESTIONS ASKED AND PARTIALLY ANSWERED

Q: WHAT IS REPLY IN CANDY FOR I/O?

(AL, STRE, WIKESFA, JOURNAL)

ANS:

COMPATIBLE W/STRECA IF IT DOESN'T COST EXTRA.

OPTIONAL KEYBOARD ~~AND~~

AND CASSETTE INTERFACE - ACCESSED THRU CONTROL PORTS.

=> WIRE POCKET PARALLEL TO VIA.

~~DO ANY SE~~

WRITER

SECUR

DATE 2/10/77

WITNESS

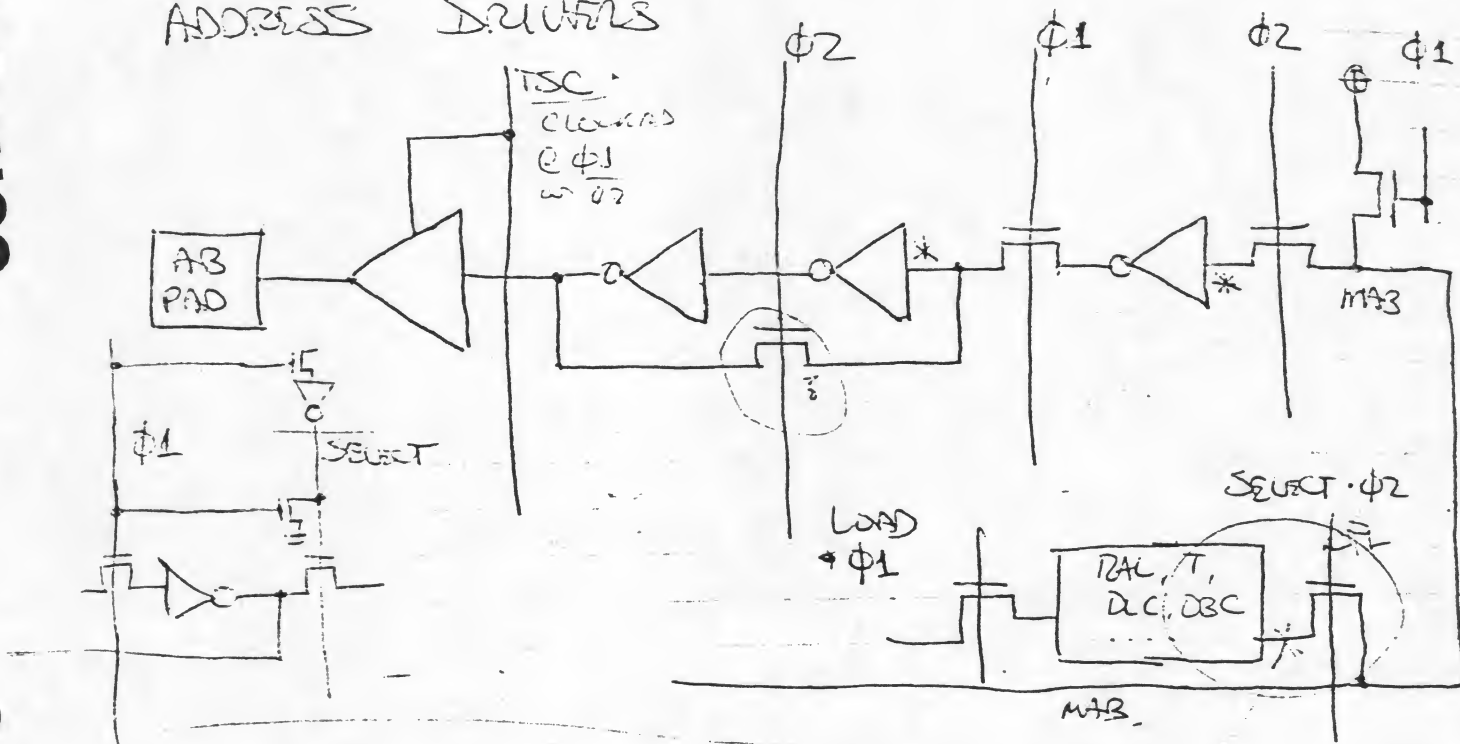
DATE

108

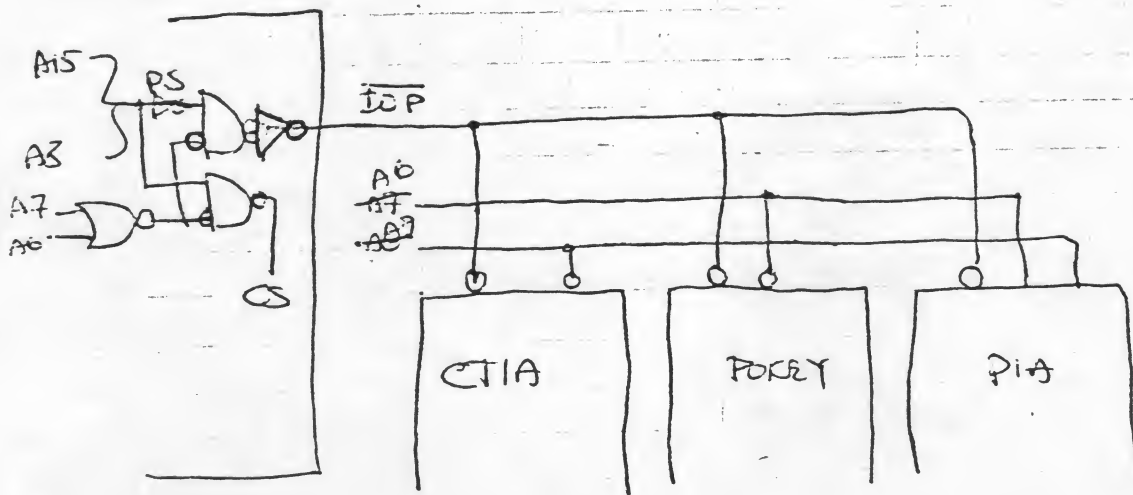
GAME OR PROJECT

ANTIC.

ADDRESS DRIVERS



CHIP SELECT SCHEME FOR COURRY/CANDY USE



ICP	A7	A6	
1	0	0	ANTIC
0	0	0	POKEY
0	0	1	CTIA
0	1	1	PIA

GAME OR PROJECT

COLLEEN/CANDY LSD PAWS

PINOUTS & INTERCONNECT.

SIGNAL	6509 (B3-2)	ANTIC	CTIA	POKET	PIA <sup>520</sup> 520
	V <sub>SS</sub> (2), V <sub>CC</sub> 3	V <sub>SS</sub> , V <sub>CC</sub> 2	V <sub>SS</sub> , V <sub>CC</sub> 2	V <sub>SS</sub> , V <sub>CC</sub> 2	V <sub>SS</sub> , V <sub>CC</sub> 2
3.58 MHz		OSC	OSC		
Φ <sub>0</sub>	Φ <sub>0</sub> IN 1	Φ <sub>0</sub> OUT 1			
Φ <sub>1</sub>	Φ <sub>1</sub> OUT 1				
Φ <sub>2</sub>	Φ <sub>2</sub> OUT 1	Φ <sub>2</sub> 1	Φ <sub>2</sub> 1	Φ <sub>2</sub> 1	Φ <sub>2</sub> 1
$\overline{RES}$	$\overline{RES}$ 1	$\overline{RES}$ 1			$\overline{RES}$ 1
$\overline{NMI}$	$\overline{NMI}$ IN 1	$\overline{NMI}$ OUT 1			
$\overline{IRQ}$	$\overline{IRQ}$ IN 1			$\overline{IRQ}$ OUT 1	$\overline{IRQA, B}$ 2
$\overline{RDY}$	$\overline{RDY}$ IN 1		$\overline{RDY}$ OUT 1		
$\overline{HALT}$	$\overline{HALT}$ IN 1	$\overline{HALT}$ OUT 1	$\overline{HALT}$ IN 1		
$\overline{IOP}$		$\overline{IOPACK}$ OUT 1	$\overline{CS}\phi$ 1	$\overline{CS}\phi$ 1	$\overline{CS}2$ 1
R/W	R/W TS 1	R/W TS 1	R/W 1	R/W 1	R/W 1
SYNC	SYNC 1				
DB0-DB7	DΦ-D7 8	DO-D7 8	DO-D7 8	DΦ-D7 8	DΦ-D7 8
AB0-AB5	AΦ-A5 6	AΦ-A5 6	AΦ-A4 5	AΦ-A3 4	RSΦ, RS1 2
AB6	A6 1	A6 1		$\overline{CS1}$ 1	1
AB7	A7 1	A7 1	$\overline{CS1}$ 1		1
AB8-AB15	A8-A15 8				
V <sub>DD</sub> SYNC		$\overline{CSYNC}$ OUT 1	$\overline{CBLANK}$ OUT 1	$\overline{CBLANK}$ OUT 1	
VIDEO CODES		AUΦ-2 OUT 3	AUΦ-2 IN 3		
LUM		LUM Φ 1	LUM Φ-2 3		
CHARACT			CHR, DEL 2		
CONTROL CODES			CCOD Φ 3 4		
AUDIO				AUDIO 1	
KEYBOARD				KSΦ-KS5, KRI, 2 8	
SPRUAL PWR.				SCLK, SDIN, SDOUT 3	
POTS				POT Φ-7 8	
JOYSTICKS IN			IN Φ-3 4		
JOYSTICKS DB					PAΦ-7, PB1-7 16
LIGHT POT		LPIN 1			
(CANDY PARALLEL)					CAΦ1, CBΦ1 4
OTHER	S.O. 1				
SPARE	nc 2		nc 1		
PANSTICK	40	40	40	40	40

WRITER DATE WITNESS DATE



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ANTIC.

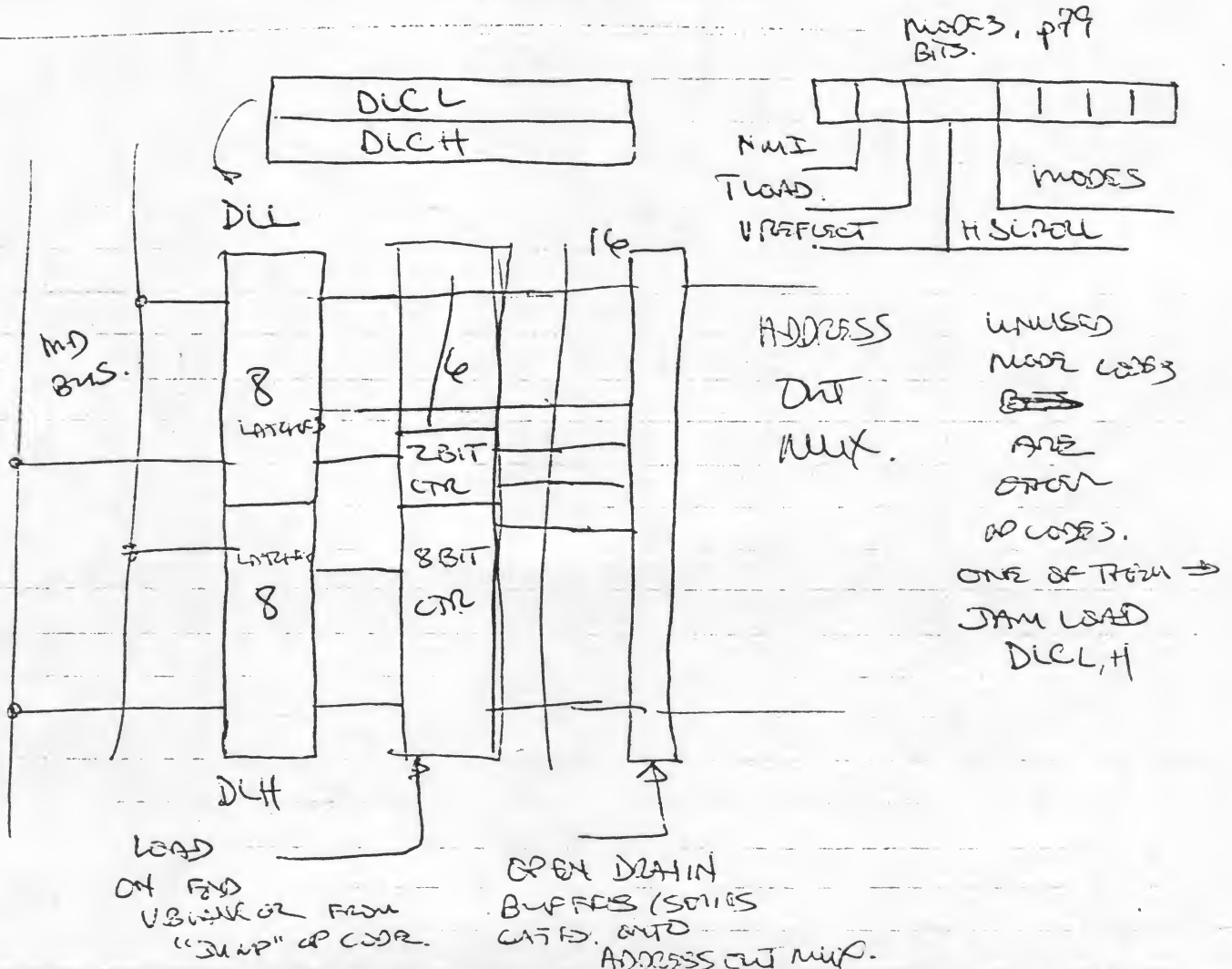
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MIKE ALBAUGH HAS CONCLUDED

JAM AFTER LUNCH THAT THE

DISPLAY LIST COUNTER SHOULD

- A) BE JAM LOADABLE.
- B) JAM LOAD REGISTER LOADED BY CPU.
- C) JAM LOADABLE BY AN OP CODE IN THE DISPLAY LIST (JUMP)



FROM LONG DISCUSSION OF VERTICAL  
SCROLLING

CONCLUSIONS FIRST

CPU CAN NOW LOAD A  $\Delta$  REGISTER

$\Delta$  REGISTER OR MODE PLA LOADED INTO  
 $\Delta$  COUNTER,

TWO STROBE LOCATIONS

- START SCROLL

$\Delta$ CTR  $\leftarrow$   $\Delta$  REG INSTEAD OF MODE PLA

- END SCROLL

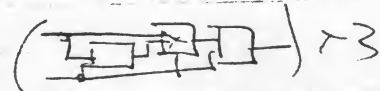
MODE FETCH REQUEST SET AT  $\Delta$ REG =  $\Delta$ CTR  
INSTEAD OF  $\Delta$ CTR =  $\emptyset$

MODE FROM ANTIC SET AT SAME TIME AS  
MODE FETCH REQUEST (1 LINE AHEAD  
OF MODE FETCH)

HORIZONTAL SCROLLING

SLIP COUNTER THAT IS SIDE LOADED  
ONCE/LINE - SCROLLS TO 1 COMPUTER  
CLOCK RESOLUTION - USED TO GENERATE  
T COUNTER AND GENERATES DMA FETCHES -

1/2 COMPUTER CLOCK (1 LINE CLOCK) SCROLLING  
INDEX WITH SIMPLE 2ND DELAY AT  
OUTPUT OF MODE/CHARS PLA - JUST BEFORE  
ANTIC OUTPUT



INVENTORY OF REGISTERS.

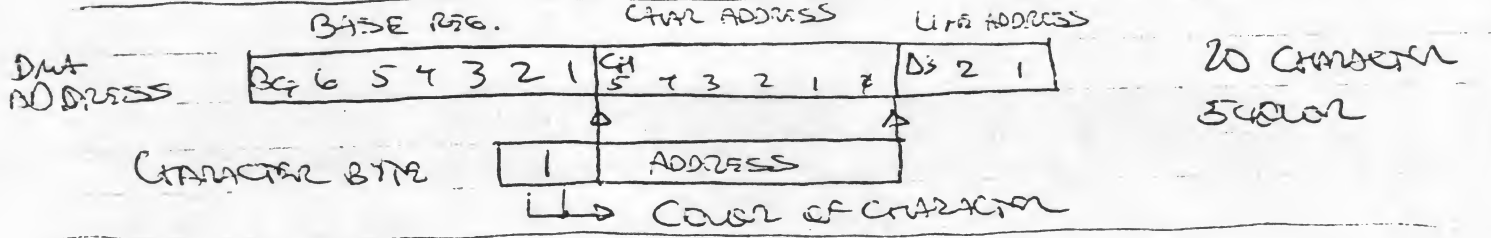
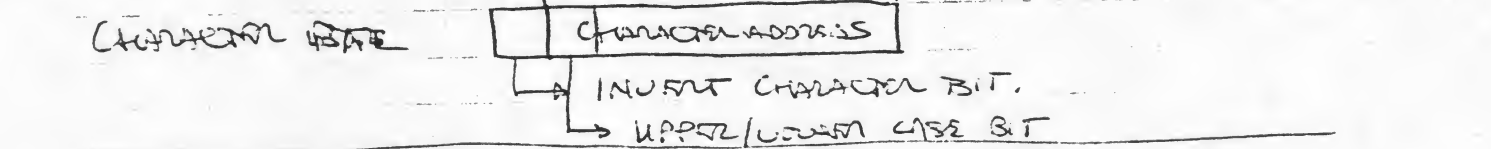
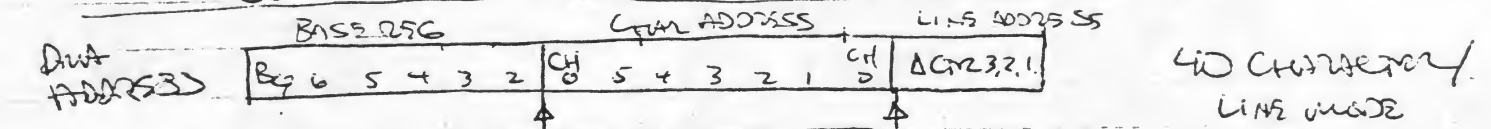
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NMI REQ	MD	VB	0	✓	READ					
NMI MASKS	MD	VB	0	✓	WRITE					
NMI ACK. VB			STROBE	✓	WRITE					
MD.			STROBE	✓	WRITE					
LP CONTROL			0	✓	WRITE					
LP STATE	V <sub>10</sub>	LP	AB	✓	READ					
HSCREEN SIZE, PECTRL	0	S	?	✓	WRITE					
VSYNC COUNTER	V <sub>7</sub>	N <sub>6</sub>	V <sub>5</sub>	V <sub>4</sub>	V <sub>3</sub>	N <sub>2</sub>	V <sub>1</sub>	V <sub>0</sub>	✓	READ
LP H	V <sub>7</sub>	-	-	-	-	-	-	V <sub>0</sub>	✓	READ
LP V	H <sub>7</sub>	-	-	-	-	-	-	H <sub>0</sub>	✓	READ
HSCREEN			#S <sub>2</sub>	#S <sub>1</sub>	#S <sub>0</sub>				✓	WRITE
ΔREGISTER VSCREEN			V <sub>2</sub>	V <sub>1</sub>	V <sub>0</sub>				✓	WRITE
START VSCREEN			STROBE	✓	WRITE					
END VSCREEN			STROBE	✓	WRITE					
INSTRUCTION REGISTER	NMI	LP	#	V	REF	MODE 3, 2, 1, 0			✓	<del>WRITE</del> DWA
CHARACTER BASE PTR	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	✓	WRITE
APC	← REG/CTR →								✓	WRITE DWA
DISPLAY LIST COUNTER	LATM								✓	"
H	- REG - CTR								✓	"
MEMORY SCAN CONTROL	CTRL								✓	<del>WRITE</del> DWA ON
H	LATM				CTR				✓	"
OBJECT SCAN CONTROL	CTR								✓	WRITE
H	LATM				CTR				✓	"
RAM ADDRESS LATM									✓	WRITE ONLY
PORT OUTPUT REGISTER	1	1	1	1	1	1	1	1	✓	DWA ONLY. OR INTRINSIC
RESET VSYNC	STROBE								✓	WRITE } FOR TESTING
RESET HSYNC	STROBE								✓	WRITE }
OBJECT SCAN ENABLE									✓	WRITE.

INVENTORY OF MODE CODES. (FROM P85)

0000	BLANK (BACKGROUND) (3BIT N) (1-8)	CTR
0001	JUMP 1 LINE BACKGROUND AND RELOAD <del>DIS</del> DISPLAY LIST	
0010	(TOUCH UPPER CASE) ?	
0011	40 CH UPPER AND LOWER CASE ?	
0100	20 CH x 5 COLOR x 8 LINES	} 20 + 70 DMA LINE
0101	20 CH x 5 COLOR x 8+2 LINES	
0110	20 CH x 4 COLOR x 8 LINES	
0111	20 CH x 4 COLOR x 8+2 LINES	
<del>(40 CELL x 2 COLOR x 8 LINES)</del>		<del>DELETED</del>
1000	40 CELL x 4 COLOR x 8 LINES	} 10 DMA LINE
1001	80 CELL x 2 COLOR x 4 LINES	
1010	80 CELL x 4 COLOR x 4 LINES	} 20 DMA LINE
1011	160 CELL x 2 COLOR x 2 LINES	
1100	160 CELL x 4 COLOR x 2 LINES	} 40 DMA LINE
1101	320 CELL x 2 LEVEL x 1 LINE	

CHARACTER ADDRESS FORMATS:



GAME OR PROJECT  
COWSTY / CANDY.

### INTERUPT STRUCTURE

RESET	—	ONLY POWER ON —	
		ALSO FIREWLD BY BREAK KEY.	
NMI	—	VIDEO INTERRUPTS.	
MASKABLE WITHIN ANTIC.	{	1. VBLANK	START VBLANK
		2. DISPLAY BLOCKS	END DISPLAY BLOCK
IRQ	—	NON VIDEO I/O	
MASKABLE ON CHIP AND IN SOURCES	{	1. KEYBOARD	FIREW KEY, BREAK KEY
		2. SERIAL PORT	RECV BYTE, SEND BYTE
		3. AUDIO TUNER.	END COUNT.
	{	4. EXTERNAL DEVICES ON EXPANSION BOX.	

~~LEFT PORT I/O NOT INTERRUPT DRIVEN,~~  
~~TRIGGER PORTS NOT INTERRUPT DRIVEN~~  
~~JOYSTICKS NOT INTERRUPT DRIVEN~~  
~~POTS NOT INTERRUPT DRIVEN~~

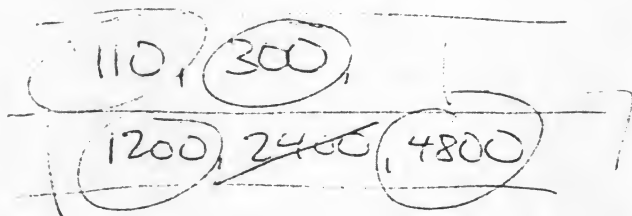
ANTIC MOSTLY DMA  
 DIA POSSIBLY DMA

JAY'S SUGGESTION - 14 DEC 77

BRING IN EXTERNAL EXPANSION INTERRUPT VIA ONE OF CA1,2, CB1,2 PORTS,

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→ JERRY SERIAL PORT DISCUSSION w/MIKE



9600, 19200

MIKE SUGGEST 16<sup>x</sup> CLOCK

DOES NOT JUST TALK TO OTHER  
ATARI PRODUCTS.

MIKE RAISES ISSUES ABOUT

CLOCK TOLERANCE - SKEWING  
IF BUFFERS ARE NOT REGENERATIVE -  
SYNCHRONOUS WITH CLOCK.

NEVER HAVE MORE THAN

ONE BAUD RATE OUT  
THREE AT ANY ONE TIME.

PERHAPS THE CLOCK SHOULD  
BE BIDIRECTIONAL.

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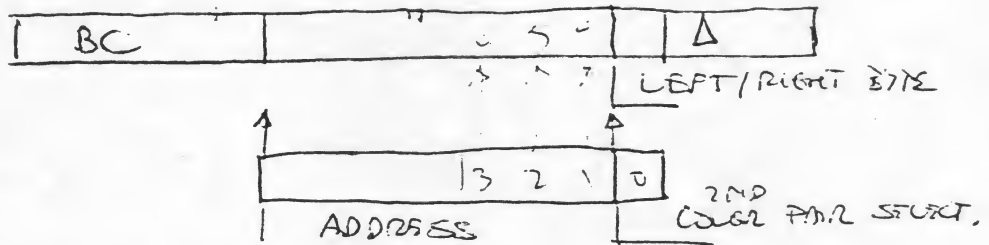
INTIC

SCOTT'S SUGGESTION

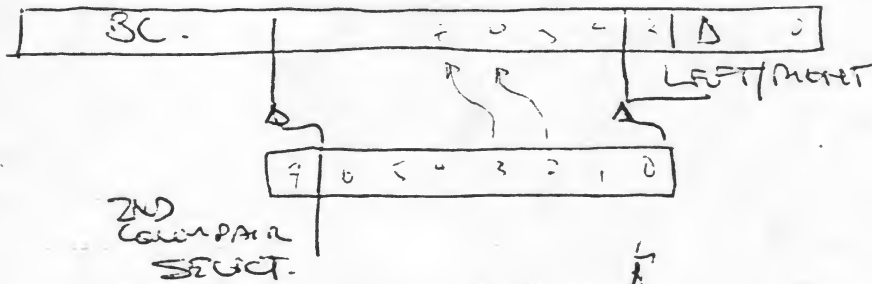
IN 20 CHARACTER X 4 COLOR

SHIFT CHARACTER UP

INSTEAD OF



SHIFT CHARACTER UP



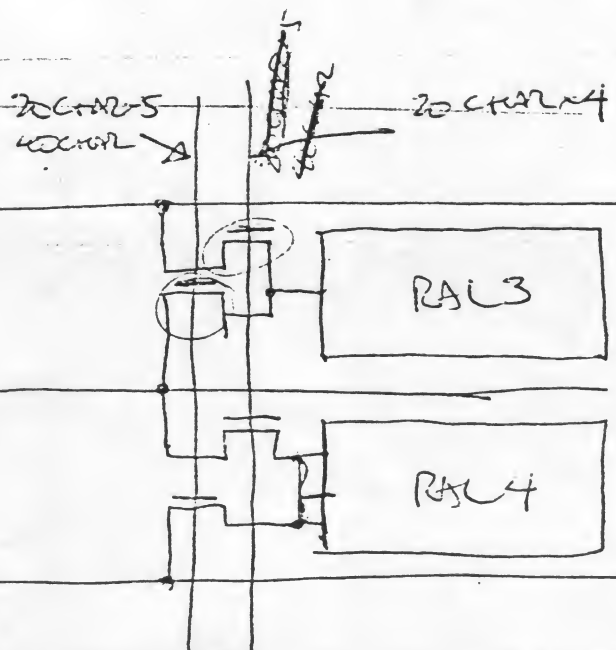
HOW TO DO IT.

EXAMPLE, RAL 2,3

MAB7

MAB6

MAB5

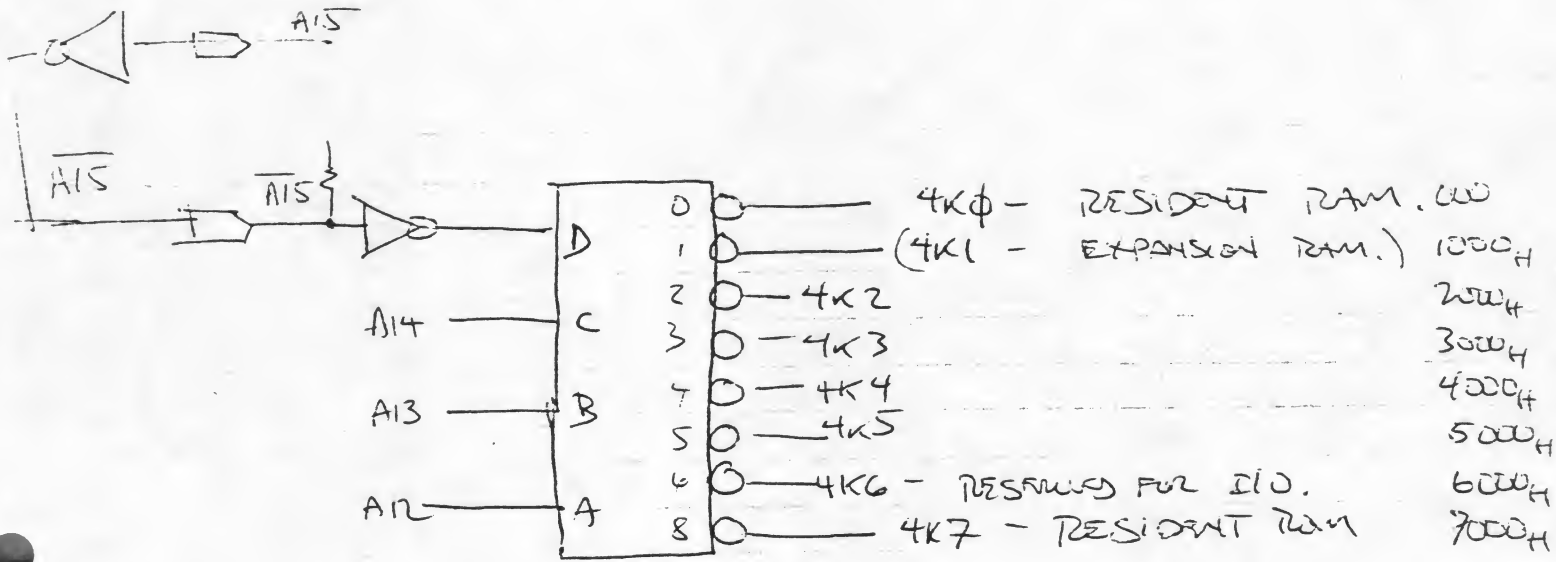


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GAME OR PROJECT  
 CONQUEST, CANDY

SUGGESTED ADDRESS DECODING SCHEME



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6 DMA SEQUENCES.

1. 40 CELL / 4 COLOR, 80 CELL / 2 COLOR.

10 DMA / LINE. 1ST LINE ONLY

LEADS BY 4 CYCLES  
4 CYCLES TOTAL  
8 CYCLES FREE

2. 80 CELL / 4 COLOR, 160 CELL / 2 COLOR

20 DMA / LINE 1ST LINE ONLY

LEADS BY 4 CYCLES  
4 CYCLES TOTAL  
4 CYCLES FREE

3. 160 CELL / 4 COLOR

40 DMA / LINE 1ST LINE ONLY.

LEADS BY 4 CYCLES  
4 CYCLES TOTAL  
20 CYCLES FREE

4.

~~20 CHARACTER / 5 COLOR~~  
20 CHARACTER / 5 COLOR

20 + 20 DMA 1ST LINE  
20 DMA / LINE THEREAFTER

LEADS BY 6 CYCLES  
6 CYCLES TOTAL  
4 CYCLES FREE

5.

20 CHARACTER / 4 COLOR

20 + 40 DMA 1ST LINE  
40 DMA / LINE THEREAFTER

LEADS BY 8 CYCLES  
8 CYCLES TOTAL  
4 CYCLES FREE

6.

40 CHARACTER / 2 COLOR

40 DMA 1ST LINE  
40 DMA / LINE THEREAFTER

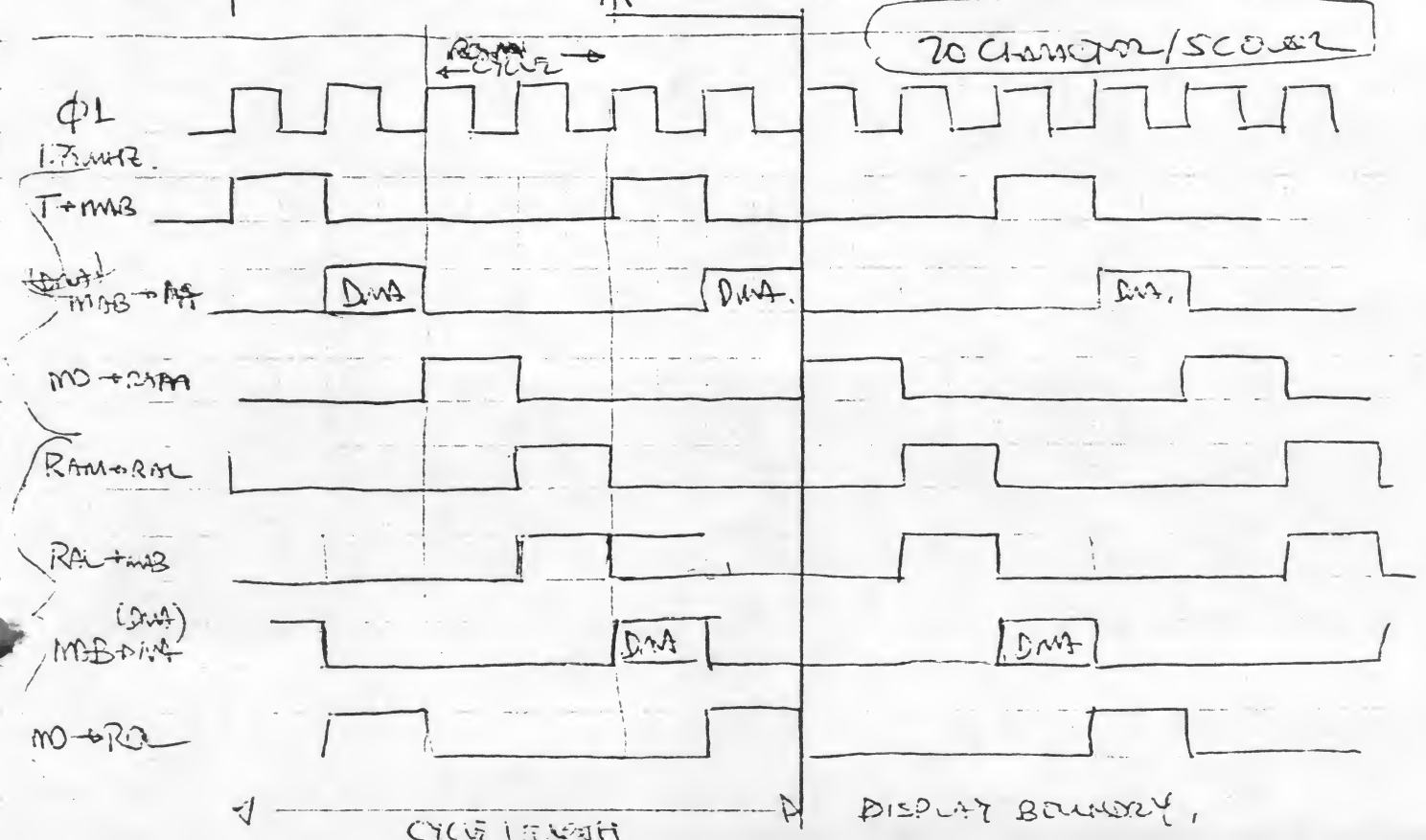
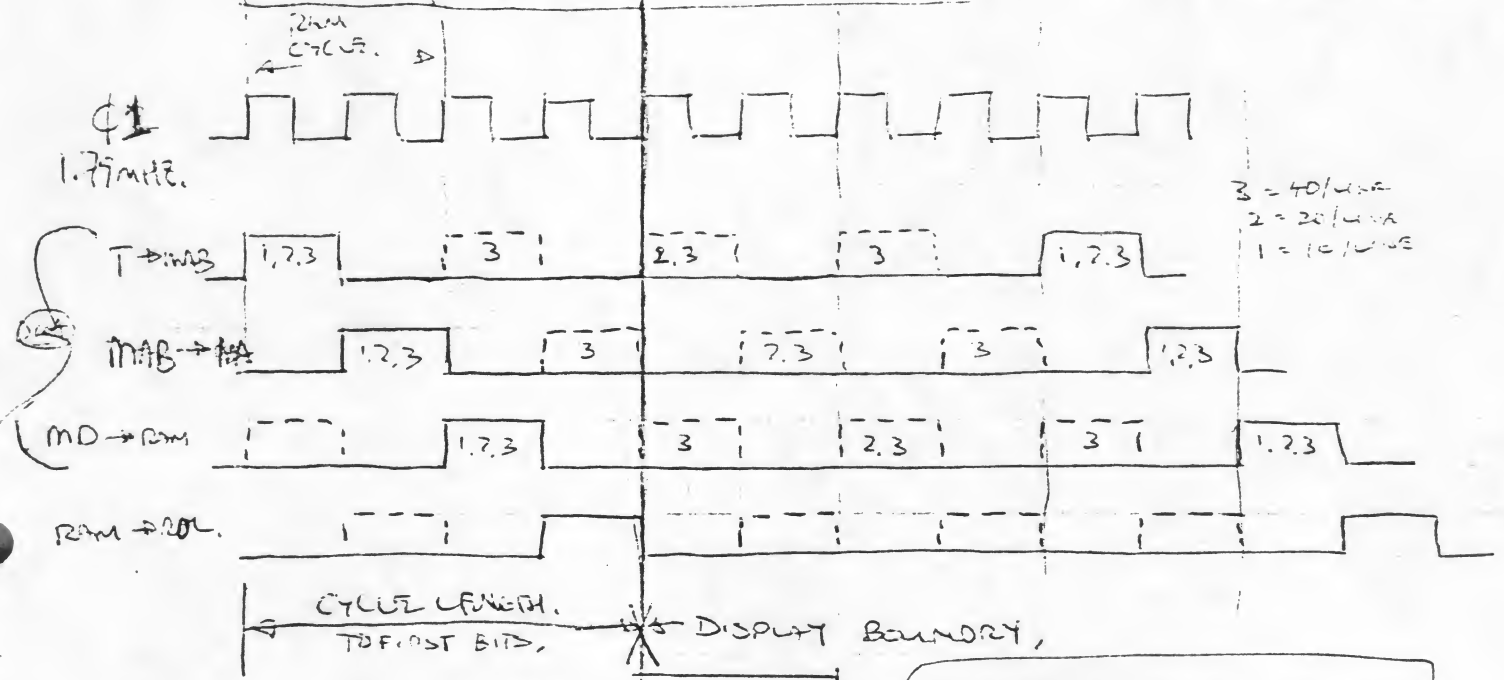
LEADS BY 6 CYCLES  
6 CYCLES TOTAL  
2 CYCLES FREE



GAME OR PROJECT: ANTC CHIP DMA TIMING INSTRUCTIONS: 20 CLOCKS

T LEADS BY 4 CYCLES. (from JAYS TIMING DIAGRAMS)

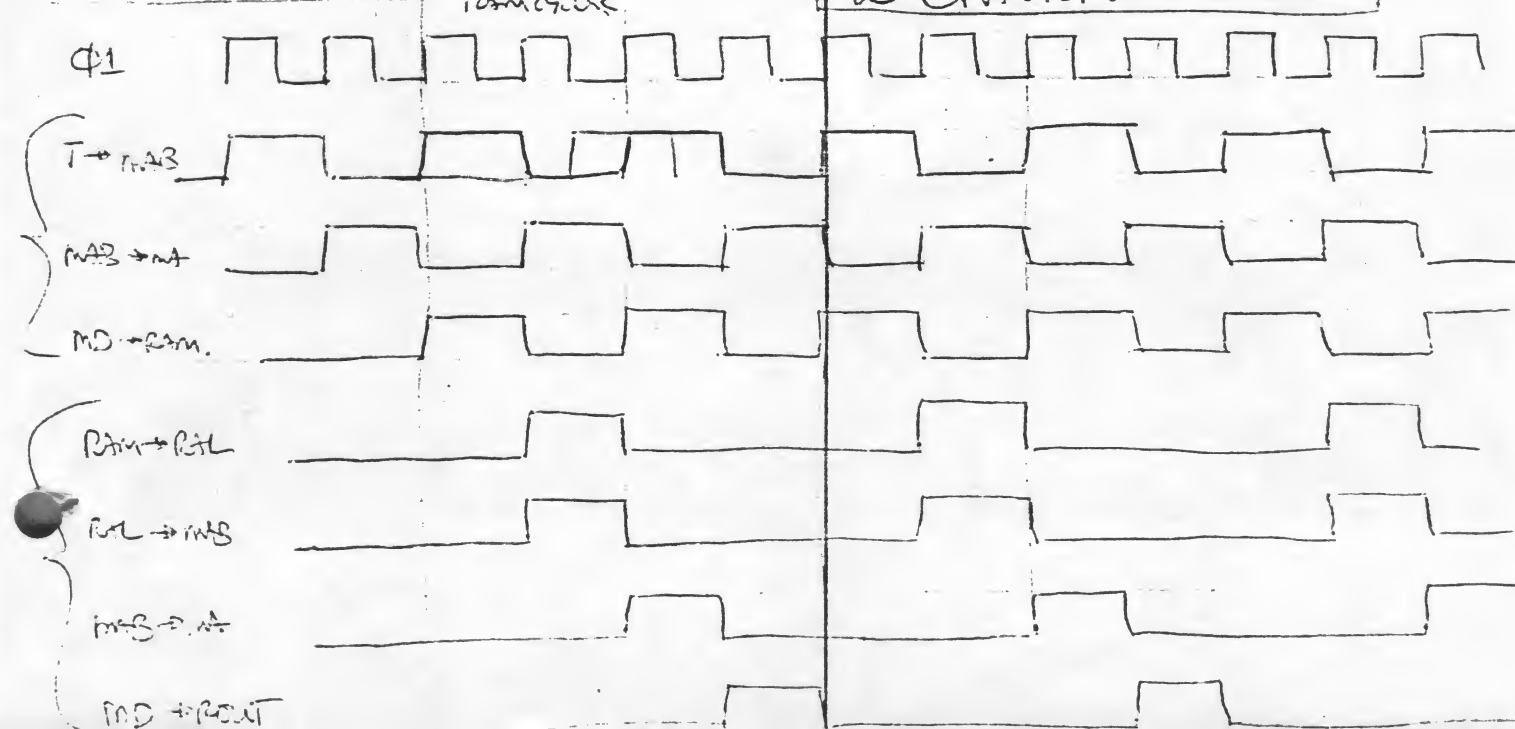
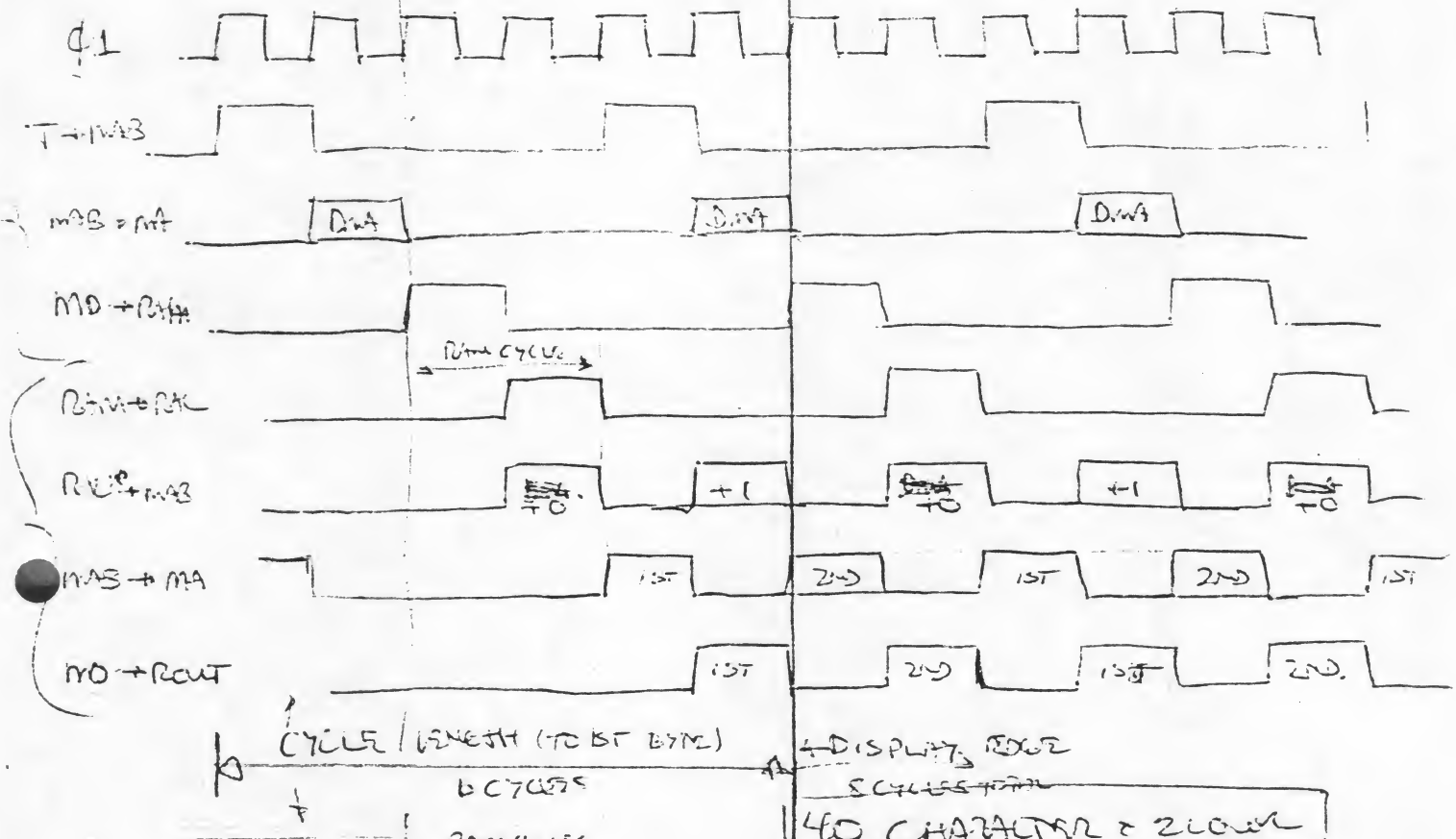
### MEMORY MAP DMA SEQUENCES

40, 80, 160 DMA/LINE


GAME OR PROJECT

ANTIC, DMA TIMING, 70 CHAR/ROW, 40 CHAR/2

(20 CHAR \* 4 ROWS)



ET

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# DESIGN of Man Computer DIALOGUES

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